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In-depth electrical characterization of deca-nanometer InGaAs MOSFET down to deep cryogenic temperatures

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Abstract—This work presents a detailed electrical characterization of planar InGaAs on Insulator MOSFETs from room temperature (namely 300 K) down to deep cryogenic temperatures (10 K). The main electrical parameters of MOSFET operation (threshold voltage V_t, low-field mobility μ_0, and subthreshold swing, SS) were extracted in both linear and saturation regions of operation through the consolidated Y-function method, for gate lengths down to 10 nm. The extracted parameters are first analyzed versus temperature and length and then compared against a more mature technology such as Silicon FDSOI MOSFETs. The results reveal competing advantages of the III-V alloy, particularly when going down to cryogenic temperatures.

Keywords— III-V, MOSFET, cryogenic, Y-function, characterization, InGaAs

I. Introduction

As the research on Quantum Computing (QC) advances , the engineering of the circuitry surrounding the quantum bits themselves requires further study. This necessity is better understood when considering the readout electronics [1] devoted to quantum computing: in order to minimize signal transmission delays and noise amplification due to different temperatures amongst signal stages, readout electronics in QC have to be as close as possible to the actual bits, therefore operating in the temperature range of a few units of Kelvins. Thanks to their enhanced mobility, III-V MOS devices can provide the same ON current at lower power supply voltages, and by turn reduced power consumption and heat dissipation, crucial at QC operation temperature. Thus, the precise identification of their electrical parameters behavior with temperature and channel length is required for reliable modeling and circuit design. On the other hand, as this technology is not as mature as its Silicon-based counterparts (Bulk, FDSOI, and FinFETs), the need of full electrical characterization down to deep cryo-temperatures, becomes challenging and critical, particularly in view of the emerging technology of QC.

To date, Silicon technology has been extensively studied and experimentally characterized [2-5], while on the other hand many modelling and simulation studies have been carried out concerning III-V alloys, particularly highlighting the conduction in satellite valleys [6].In this work, we study InGaAs MOS devices so as to compare the effects due to both channel length and temperature reduction with those already known for Si [5], particularly to see if the same physical limits apply as in the case of subthreshold swing settling [2]. Moreover, we tried to position our characterization work with respect to results from transport simulation and to see how these impact the ease of parameter extraction.

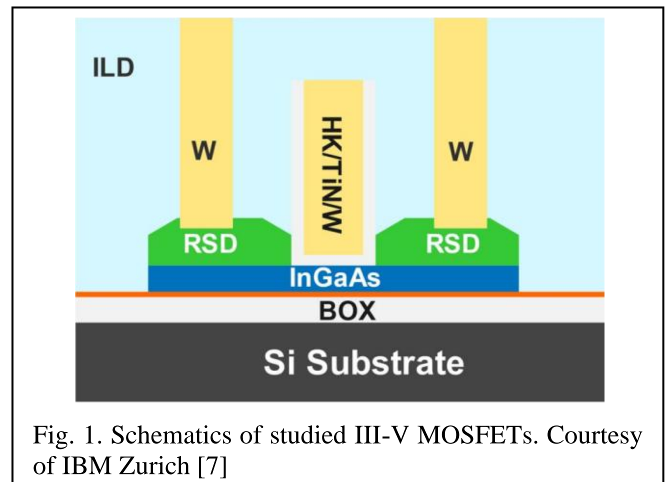

Fig. 1. Schematics of studied III-V MOSFETs. Courtesy of IBM Zurich [7]

II. Devices under study and Extraction methodology

The devices under test were fabricated by IBM Zurich [7], based on a III-V on insulator tehnology, incorporating a 20 nm InGaAs film, insulated by a buried oxied and handled through a Silicon substrate (Fig.1). They share a common gate width value of W = 1 μm and channel lengths spanning from L = 300 down to 10 nm. The measurements were carried out at wafer level down to 10K using a HP 4155A parameter analyzer and a Formfactor SussTech 300mm Cryo probe station.

In order to extract the main parameters that define the MOSFET performance, we utilized the Y-function method, expressed through $Y(V_g) = I_d/\sqrt{g_m} \approx \sqrt{\beta}(V_g - V_t)$ [8], where $\beta = W\mu_0 C_{ox} V_d / L$. This function suppresses any access resistance effect and thanks to its linear behavior versus V_g at

strong inversion, the linear fit can provide the threshold voltage, V_t, as well as the low-field mobility, μ_0, value through the x-axis intercept and slope, respectively.

III. Experimental Results and Discussion

A. Preliminary observations

The measured I_d-V_g input characteristics in linear regime are plotted in Fig. 2a, for the two temperature limits (10 K and 300 K). Through a first glance, we can already observe how the threshold voltage, V_t, is affected by both channel length and temperature: on one hand, for a shorter channel V_t shifts downwards ("V_t roll-off" short channel effect), while on the other hand, it increases for a decreasing temperature.

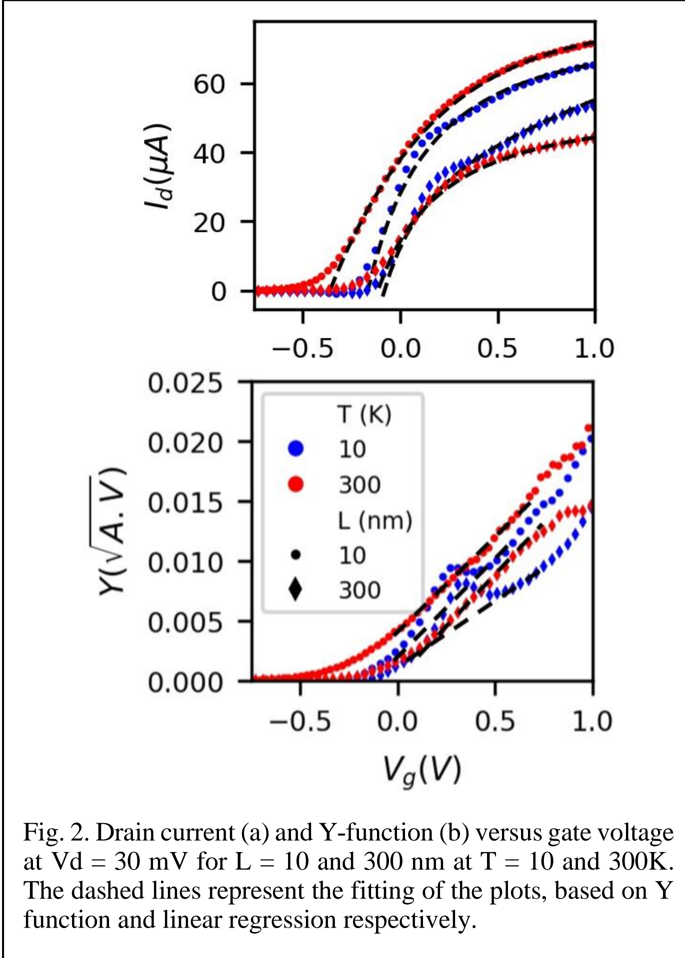

Fig. 2. Drain current (a) and Y-function (b) versus gate voltage at Vd = 30 mV for L = 10 and 300 nm at T = 10 and 300K. The dashed lines represent the fitting of the plots, based on Y function and linear regression respectively.

Moreover, we can notice some kind of a shoulder/hump in the high V_g region, in both the I_d-V_g and the Y-V_g (Fig. 2b) curves: this effect is most likely to be related to the onset of conduction in the L valley [6] of III-V. What is most important for our study, however, is that this hump does not impact the overall linear behavior of the Y function in strong inversion, allowing us therefore an easy and reliable extraction of the main operation parameters.

B. Analysis of extracted parameters in ohmic region

When going down to low temperatures (LT), several effects are taking place. First, due to the Boltzmann statistics, as the temperature decreases, fewer and fewer electrons are promoted to the conduction band for the same gate voltage . This is reflected in an increase in threshold voltage as going towards lower temperatures, as shown in the extracted V_t values, plotted versus temperature for all measured gate lengths in Fig. 3. This increase at low temperatures reaches a maximum V_t value, which corresponds to the degenerated behavior of the semiconductor at that range of temperatures .

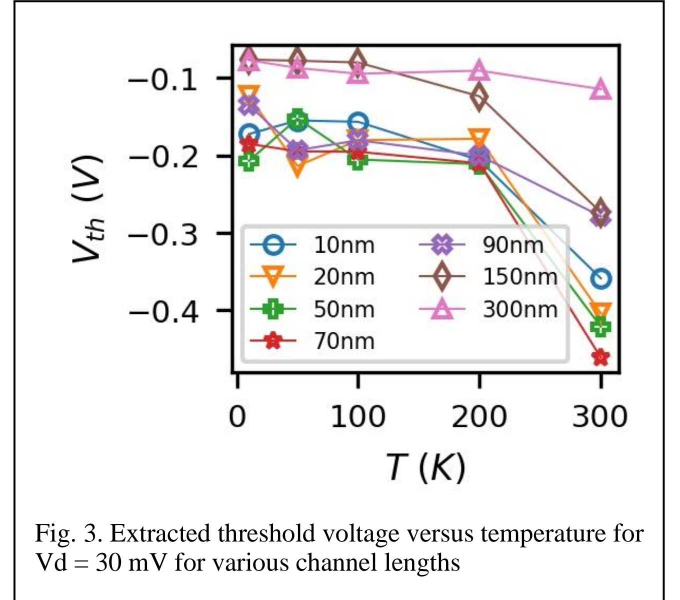

Fig. 3. Extracted threshold voltage versus temperature for Vd = 30 mV for various channel lengths

Moreover, the transition between OFF and ON states becomes sharper (Fig. 4), yielding a consequent decrease of the subtreshold swing, SW, for low temperatures, down to a settling value of about 10 mV/dec, which is attributed to the exponential band tails of states [2]. This behavior of SW is confirmed for the measured III-V devices, as shown in Fig. 5, where the extracted values of SW are plotted versus temperature for certain channel lengths.

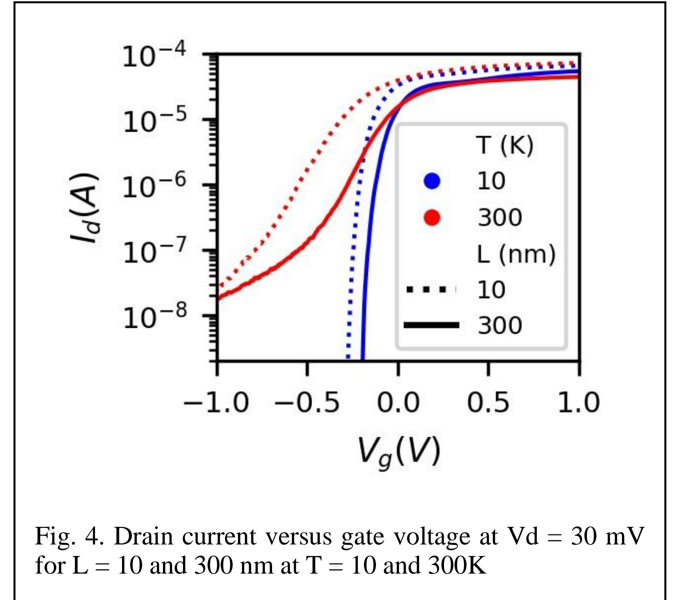

Fig. 4. Drain current versus gate voltage at Vd = 30 mV for L = 10 and 300 nm at T = 10 and 300K

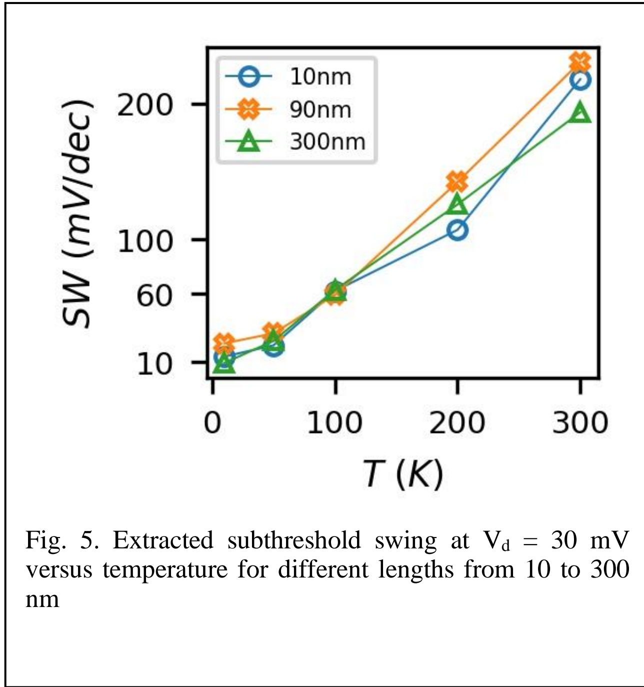

Fig. 5. Extracted subthreshold swing at V_d = 30 mV versus temperature for different lengths from 10 to 300 nm

Conversely, as the temperature lowers, there is less and less vibrational energy in the lattice, causing a decrease in phonon scattering , which allows an increase in the low-field mobility, μ_0, as shown in a, where the extracted values of μ_0 are plotted versus temperature for all measured gate channel length. This increase is evidently more pronounced in longer channel devices, whereas, in shorter channels, defect (neutral impurity) scattering is prevailing due to source/drain regions proximity , yielding a generally lower mobility and also a less significant increase at lower temperatures [5].

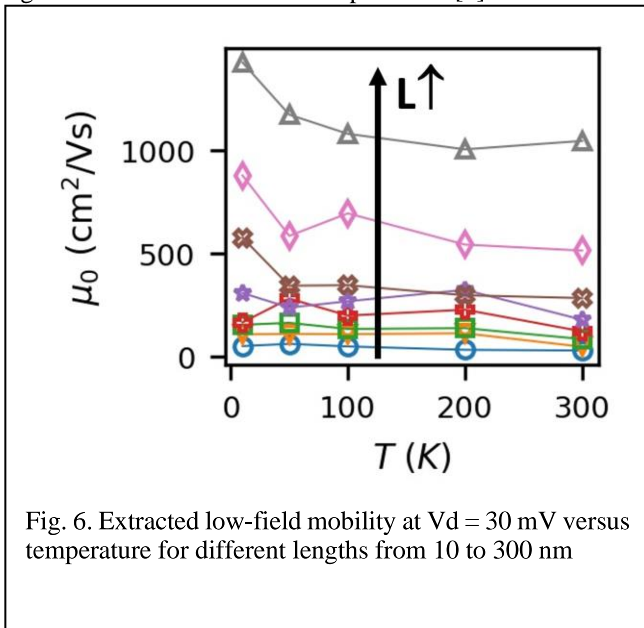

Fig. 6. Extracted low-field mobility at Vd = 30 mV versus temperature for different lengths from 10 to 300 nm

As it can be shown through Poisson-Schrodinger simulations [ref Oregan I ref list], the effect of L valley carrier population becomes opnly visible below 100K, giving rise to specific structure in Id-Vg and Y-Vg characteristics (Fig. 2).

C. *Behavior in saturation region*

As we proceed towards the analysis of the device parameters in saturation region of operation (V_d = 1 V), we observe that both 10 and 300 nm length devices, plotted in Fig. 7, show no significant variation as going to low temperatures.

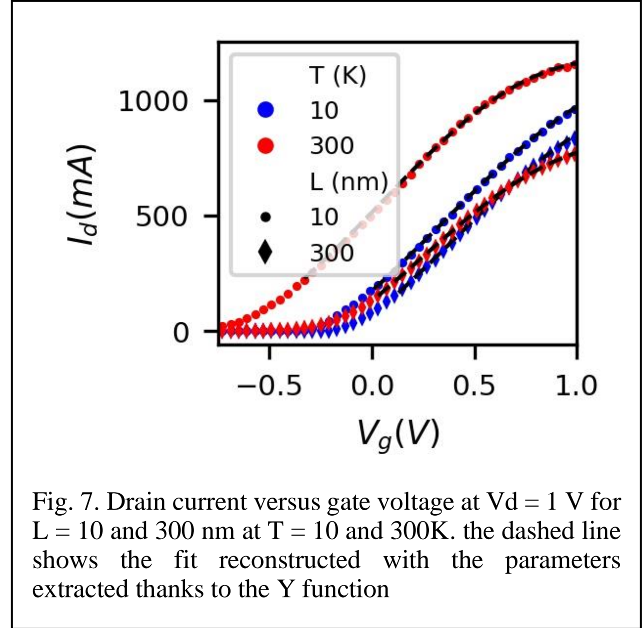

Fig. 7. Drain current versus gate voltage at Vd = 1 V for L = 10 and 300 nm at T = 10 and 300K. the dashed line shows the fit reconstructed with the parameters extracted thanks to the Y function

From the consequent extraction, the variation of both V_t and SW parameters with respect to temperature in the saturation region is very small. On the contrary, we notice that in saturation region, the curvature created by the takeover of L valley is no longer visible at low temperature. This can be explained when considering that the drain current is obtained by integration along the channel from source to drain [9]: close to the drain region the influence of high V_d does not allow the quasi Fermi level to fill the L valley, thus attenuating its effect.

When extracting the μ_0 values through Y function, plotted in Fig. 8, compared to the linear region, the devices present a μ_0 reduction due to velocity saturation (v_{sat}) effect [3]. Moreover, it is worth noticing how the extracted mobility never reaches the ballistic limit [4], revealing that the exponential behaviour of μ_0 with respect to channel length is in fact scattering-related. The extracted values of v_{sat} in saturation region are plotted in Fig. 9, showing a good stability with respect to temperature and a slight increase for a decreasing channel length due to overshoot effect .

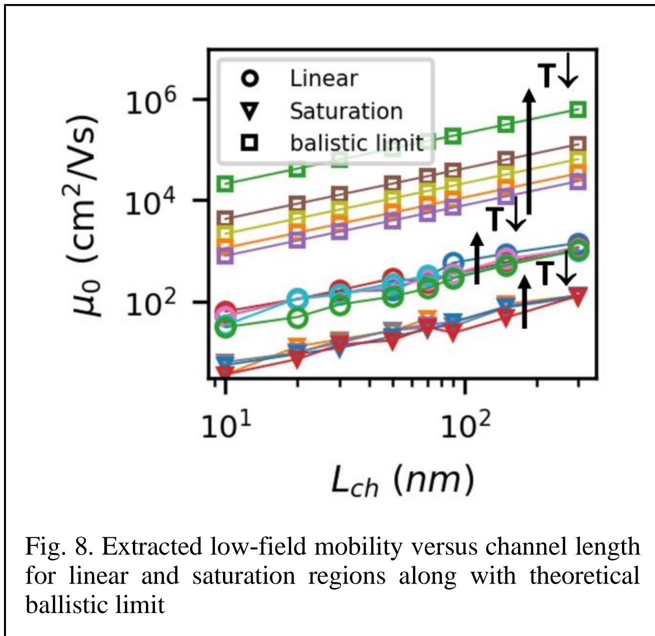

Fig. 8. Extracted low-field mobility versus channel length for linear and saturation regions along with theoretical ballistic limit

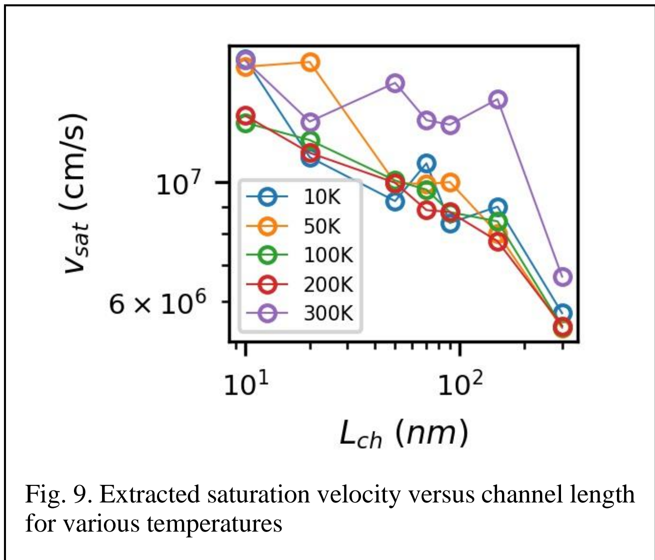

Fig. 9. Extracted saturation velocity versus channel length for various temperatures

D. Benchmarking III-V against Si for Cryo

Fig. 10 illustrates the extracted parameters of μ_0, SW and v_{sat} along with respective extractions done for Si [5] channel Fully Depleted (FD) SOI MOSFETs. When comparing the R&D-level III-V devices to this more mature and industrial Si technology like FDSOI (Fig. 10) [5], we note that although SW is much higher for III-V at 300K, both technologies reach the lowest limit value at 10K. Moreover, despite the higher interface trap density at the Al_2O_3 interface, III-V shows higher μ_0 and v_{sat} at all temperatures, revealing a great III-V potential for cryo-related applications with further technology developments and the chance to overperform Si FDSOI in certain cases.

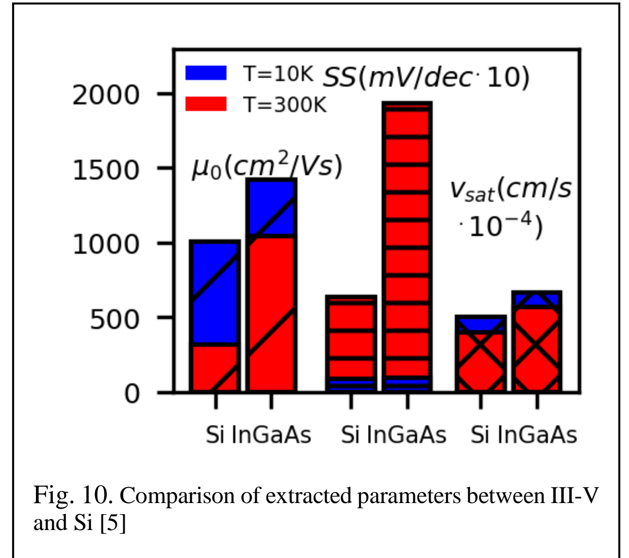

Fig. 10. Comparison of extracted parameters between III-V and Si [5]

IV. Conclusion

We have performed a detailed electrical characterization of planar InGaAs on Insulator MOSFETs from room temperature down to deep cryogenic temperatures (10K). The main MOSFET parameters (threshold voltage V_t, low-field mobility μ_0, and subthreshold swing, SS) were extracted in linear region of operation using the consolidated Y-function method for gate lengths down to 10 nm, despite the possible presence of L-valley conduction. The saturation velocity was also extracted and analysed for all lengths and temperatures. The extracted parameters of the III-V devices follow the expected behavior with temperature as in Si, while demonstrating competing advantages as compared to Si MOSFETs, particularly when going down to cryogenic temperatures.

Acknowledgment

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