Modelling of self-heating effect in FDSOI and bulk MOSFETs operated in deep cryogenic conditions

Gérard Ghibaudo, M. Cassé, F. Serra Di Santa Maria, C. Theodorou, Francis Balestra

► To cite this version:

Gérard Ghibaudo, M. Cassé, F. Serra Di Santa Maria, C. Theodorou, Francis Balestra. Modelling of self-heating effect in FDSOI and bulk MOSFETs operated in deep cryogenic conditions. Solid-State Electronics, 2022, 10.1016/j.sse.2022.108265 . hal-03852787

HAL Id: hal-03852787
https://hal-cnrs.archives-ouvertes.fr/hal-03852787

Submitted on 28 Nov 2022

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire HAL, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Accepted to Solid State Electronics (2022)

Modelling of self-heating effect in FDSOI and bulk MOSFETs operated in deep cryogenic conditions

G. Ghibaudo[1], M. Cassé[2], F. Serra di Santa Maria[1], C. Theodorou[1], F. Balestra[1],

1) IMEP-LAHC, Université Grenoble Alpes, MINATEC/INPG, 38016, Grenoble (France)
2) Université Grenoble Alpes, MINATEC/CEA, LETI, 38000 Grenoble (France)
Email: gerard.ghibaudo@grenoble-inp.fr

Abstract

A detailed analysis of the self-heating effect measured by gate thermometry in FDSOI MOSFETs is conducted in deep cryogenic conditions, showing the linear temperature dependence of the differential thermal conductance over a wide range. Then, an analytical formulation of the self-heating temperature rise as a function of power and ambient temperature in FDSOI and bulk MOSFETs valid down to very low temperatures is proposed for the first time. This self-heating temperature rise model is then used to develop an original compact model for the self-heated drain current in FDSOI MOSFETs operated down to very low temperatures.

Keywords: Self-heating effect, MOSFET, modelling, cryogenic temperature.

1. Introduction

In FDSOI devices or multi-gate field effect transistors like FinFETs and nanowire FETs, low thermally conductive materials such as the buried oxide (BOX) or the thin Si layer constituting the channel impede the dissipation of the heat generated in the channel. Consequently, the channel temperature can significantly rise when the device is in operation condition. This self-heating effect (SHE) can in turn severely affect the device performance, by reducing the carrier mobility, shifting the threshold voltage [1] or degrading the device reliability [2, 3], with implications in circuits operation [4]. The thermal effects play a more fundamental role in cryogenic electronics as the temperature increase due to SHE can be of the same order or even higher than the ambient temperature in FDSOI [5] and even in bulk MOSFETs [6]. Furthermore, at very low temperature (well below 1K), the cooling power drops down drastically (typically, 1W at 1K, 1mW at 100mK), such that the thermal management becomes more drastic. In this context, the study of self-heating effects at cryogenic temperatures provides valuable information for performance optimization. Moreover, to be accurate at cryogenic temperatures, models should take into account these thermal effects, as the device temperature can deviate significantly from the ambient one.

Therefore, in this work, we first perform a detailed analysis of the self-heating effect measured by gate thermometry in FDSOI MOSFETs in deep cryogenic conditions, showing the linear temperature dependence of the differential thermal conductance over a wide range. Then, we propose for the first time an analytical formulation of the self-heating temperature rise ΔT as a function of power and ambient temperature in FDSOI and bulk MOSFETs valid down to very low temperatures. This self-heating ΔT-model is then used to develop an original compact model for the self-heated drain current in FDSOI MOSFETs operated down to deep cryogenic temperatures, and which could easily be generalized to any other device compact model efficient in such conditions.

2. Self-heating temperature rise modelling

The experimental evaluation of self-heating was performed previously by using the conventional DC technique based on gate resistance thermometry in FDSOI MOSFETs [5]. A 2-terminal gate structure was used to measure the gate resistance Rg vs ambient temperature. By varying the ambient temperature T from 4.2 K up to 300 K, the change in the electrical gate resistance was measured as a function of the input power $P=I_d \times V_d$. The temperature rise ΔT in the device was deduced from the temperature dependence of Rg measured at zero power i.e. without self-heating effect [5]. Details of the experimental conditions and procedures can be found elsewhere [5].

Typical variations of the self-heating temperature rise ΔT with power P are shown in Fig. 1 for various ambient temperatures. Note the strong sub linearity of ΔT(P) characteristics as the ambient temperature is lowered, which is a specific feature of cryogenic operation. As explained in [5], the

temperature rise characteristics ΔT(P) can then be used to evaluate the so-called differential thermal resistance R_{th}* from the local slope as R_{th}*=δΔT/δP. Typical evolutions of R_{th}* with device temperature (T+ΔT) are shown in Fig. 2 as obtained for various ambient temperatures. These variations can be well fitted by a single expression of the form [5],

$$R_{th}{}^{*} = \frac{A}{1+\frac{T+\Delta T}{T_0}}, \quad (1)$$

where A≈8×10^4 K/W is an amplitude factor and T_0≈60K a characteristic temperature, in this case. The validity of Eq. (1) can be directly confirmed by plotting the reciprocal differential thermal resistance 1/R_{th}* i.e. the differential thermal conductance G_{th}*=δP/δΔT versus device temperature (T+ΔT) as shown in Fig. 3 for several ambient temperatures varying from T=4.2K up to 200K. Actually, it appears clearly that G_{th}* varies linearly with the device temperature (T+ΔT) over a wide range, whatever the ambient temperature used for the measurements, except maybe at temperature below 20K where the fit becomes less accurate.

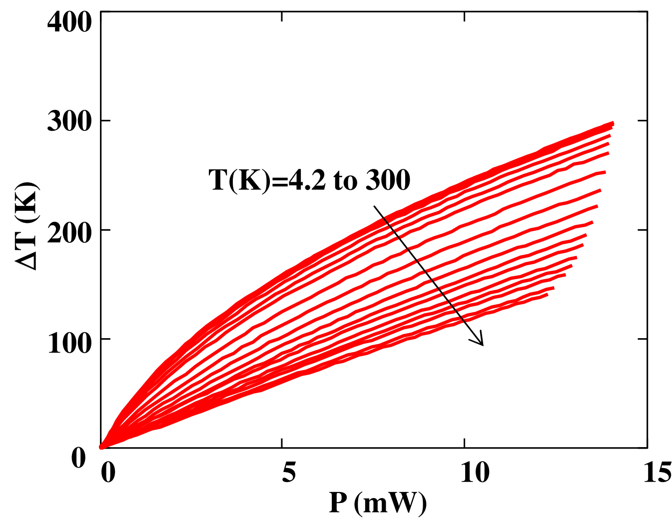


Fig. 1. Variations of temperature rise ΔT with device poser P as measured by gate thermometry in FDSOI MOS devices for various ambient temperatures T = 4.2, 6.5, 10, 15, 20, 30, 40, 50, 60, 80, 100, 120, 140, 160, 180, 200, 220, 240, 280 and 300 K (W=10µm, L=50nm, t_{si}=11nm and t_{box}=145nm). After [5].

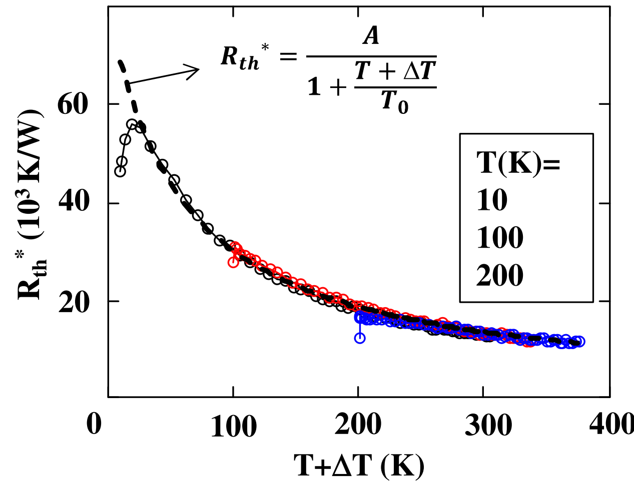


Fig. 2. Variation of differential thermal resistance R_{th}* with device temperature T+ΔT as extracted from ΔT(P) data of Fig. 1 for various ambient temperatures T=10, 100 and 200 K (W=10µm, L=50nm, t_{si}=11nm and t_{box}=145nm). After [5].

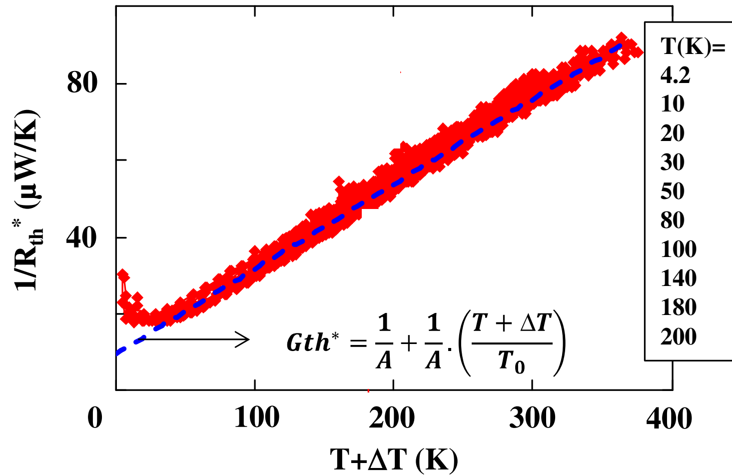


Fig. 3. Variation of differential thermal conductance G_{th}*(=1/R_{th}*) with device temperature T+ΔT for various ambient temperatures (W=10µm, L=50nm, t_{si}=11nm and t_{box}=145nm). Data after [5]. The blue dashed line shows the linear trend of the differential thermal conductance G_{th}* versus (T+ΔT) with A=8×10^4K/W and T_0=60K.

As proposed in [5], an implicit relation between power P and temperature rise ΔT can be obtained by integration of the reciprocal differential thermal resistance as,

$$P = \int_0^{\Delta T} \frac{dx}{Rth^*(T+x)} = \int_0^{\Delta T} G_{th}{}^*(T+x)dx \,. \tag{2}$$

This formulation has been used to properly fit the ΔT(P) characteristics of Fig. 1 as in [5, Fig. 6b]. However, this relation is not useful for compact modelling purpose as providing P as a function of ΔT

and T. Therefore, here we go one step further and assume that G_{th}* varies linearly with (T+ΔT), such that Eq. (2) can be integrated analytically, yielding the relation,

$$P = \frac{A.T_0}{2}.\left\{\left(\frac{1}{A} + \frac{T+\Delta T}{A.T_0}\right)^2 - \left(\frac{1}{A} + \frac{T}{A.T_0}\right)^2\right\}. \quad (3)$$

Then, after solving Eq. (3) for the variable ΔT, we obtain an explicit dependence of the self-heating temperature rise ΔT as a function of power P and ambient temperature T given by,

$$\Delta T(P,T) = \left\{\sqrt{\frac{2A.P}{T_0} + \left(\frac{T}{T_0} + 1\right)^2} - 1\right\}.T_0 - T. \quad (4)$$

This model of the self-heating temperature rise can be used to fit the ΔT(P,T) data of Fig. 1 as displayed in Fig. 4. As a result, a good agreement between experiment and modelling is found over a wide range of ambient temperature and dissipated power, thus validating the self-heating temperature rise model of Eq. (4) for FDSOI MOSFETs operated down to deep cryogenic temperatures. Note that, in the low power regime, the self-heating temperature rise takes the usual form ΔT(P,T)≈A.P/(1+T/T_0)≈R_{th}*(T).P, previously used in device modelling.

This approach can also be applied to the ΔT(P,T) data obtained by gate thermometry on bulk 40nm CMOS devices recently reported by Hart et al [6] and shown in Fig 5 (red solid lines). They found that the differential thermal resistance deduced from ΔT(P,T) data can also be fitted by an equation of the form,

$$R_{th}{}^* = \frac{A}{1+\left(\frac{T+\Delta T}{T_0}\right)^n}, \quad (5)$$

where A≈3.7×10^6 W/K, T_0=4.2K and n=2.8. Hart et al [6] also used the model of Eq. (2) with Eq. (5) to fit their ΔT(P,T) characteristics from 300K down to 4.2K (see Fig. 15 in [6]).

Following the above-mentioned approach, we can integrate Eq. (2) using Eq. (5) and obtain for the power the dependence on ΔT as,

$$P = \Delta T + \frac{T_0.\left(\frac{T+\Delta T}{T_0}\right)^{n+1}}{A.(n+1)} - \frac{T_0.\left(\frac{T}{T_0}\right)^{n+1}}{A.(n+1)}. \quad (6)$$

Contrary to Eq. (3), Eq (6) cannot be solved analytically for the variable ΔT. Therefore, we make the approximation that the "1" in the denominator of Eq. (5) can be neglected, which is equivalent to supress the first term "ΔT" in the right-hand side of Eq. (6). This assumption is true for T+ΔT>>T_0, i.e. here for T+ΔT>>4.2K. By this way, the variable ΔT can be solved and obtained analytically as a function of power P and ambient temperature T as,

$$\Delta T(P,T) = T_0.\left\{\frac{(n+1).A}{T_0}.P + \left(\frac{T}{T_0}\right)^{n+1}\right\}^{\frac{1}{n+1}} - T. \quad (7)$$

Fig. 5 shows that the self-heating temperature rise model of Eq. (7) reproduces reasonably well the ΔT(P,T) data of [6] for 40nm bulk MOSFETs operated at deep cryogenic temperatures.

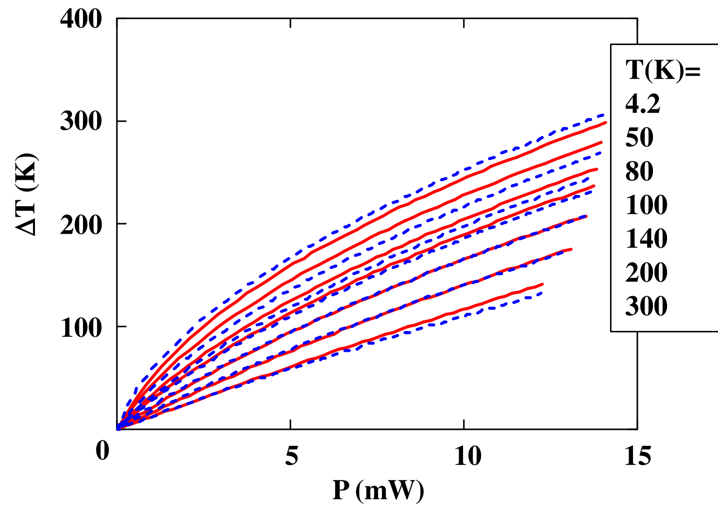


Fig. 4. Experimental (red solid lines) and modeled (blue dashed lines) variations of temperature rise ΔT with device power P in 28nm FDSOI nMOS devices for various ambient temperatures T (Fitting parameters: $A=8\times10^4$K/W and T_0=60K). Data after [5].

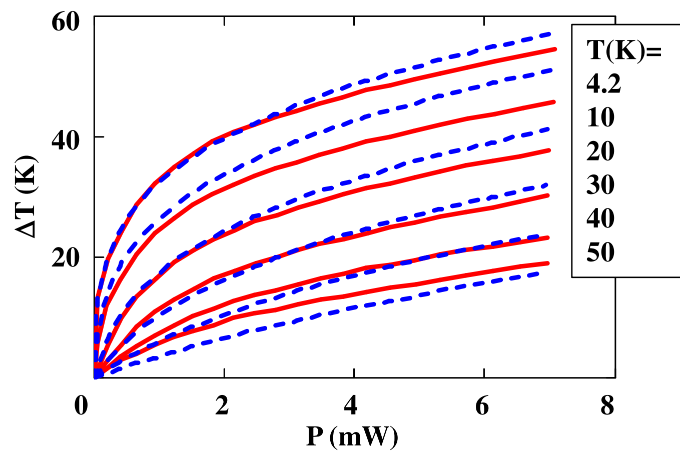


Fig. 5. Experimental (red solid lines) and modeled (blue dashed lines) variations of temperature rise ΔT with device poser P in 40nm bulk nMOS devices for various ambient temperatures T (Fitting parameters: $A=3\times10^6$K/W, T_0=4.7K and n=2.8). Data after [6, Fig. 7].

3. Self-heating MOSFET characteristic modelling

In section 2, an analytical model of SHE temperature rise ΔT(P,T) has been developed and has to be implemented in a drain current MOS device model to build up a self-heated drain current model.

Therefore, for the modelling of self-heating effect on the MOS device operation, we employ the Lambert-W (LW) function FDSOI MOSFET model first developed at room temperature [7] and recently validated from 300K down to T=4.2K for 28nm FDSOI MOSFETs in linear region [8]. In this model, the output conductance g_d is first calculated as a function of drain voltage V_d as [7,8]:

$$g_d(V_g, V_d, T) = \frac{W}{L}.\mu_{eff}(Q_i).Q_i(V_g, V_d, T), \tag{8}$$

where the inversion charge Q_i is described by the LW function as,

$$Q_i(V_g, V_d, T) = \frac{C_{ox} nkT}{q}.LW(e^{\frac{V_g - V_t - V_d}{nkT/q}}), \tag{9a}$$

$$Q_i(V_g, V_d, T) \approx \frac{C_{ox} nkT}{q}.Ln\left(1 + e^{\frac{V_g - V_t - V_d}{nkT/q}}\right).\left[1 - \frac{Ln\left[1 + Ln\left(1 + e^{\frac{V_g - V_t - V_d}{nkT/q}}\right)\right]}{1 + Ln\left(1 + e^{\frac{V_g - V_t - V_d}{nkT/q}}\right)}\right] \tag{9b}$$

and the effective mobility $\mu_{eff}(Q_i)$ takes the classical form,

$$\mu_{eff}(Q_i) = \frac{\mu_0}{1 + \theta_1 (Q_i/C_{ox}) + \theta_2 (Q_i/C_{ox})^2} \tag{10}$$

where kT/q is the thermal voltage, C_{ox} the gate oxide capacitance, n the subthreshold slope ideality factor, V_t the threshold voltage, μ_0 the low field mobility, θ_1 and θ_2 are first order and second order mobility attenuation coefficients.

Then, the drain current in common source configuration is evaluated within the gradual channel approximation by integration of the output conductance versus quasi-Fermi level varying from zero to V_d as:

$$I_d(V_g, V_d, T) = \int_0^{Vd} g_d(V_g, u, T) du. \tag{11}$$

Noting that, for the LW-function model of Eq. (9), we have $dQ_i/dV_d = q.n.C_{ox}.Q_i/kT/(C_{ox} + q.Q_i/kT)$, yields, after changing the variable of integration V_d by Q_i in Eq. (11), the analytical expression for the drain current:

$$I_d(V_g, V_d, T) = \frac{W}{L}.\mu_0.\frac{kT}{q}.n.\left[\begin{array}{l} \frac{1}{2}.\frac{C_{ox}}{\theta_2 n.kT/q}.ln\left(\frac{1 + \frac{\theta_1}{C_{ox}}.Q_{iS} + \frac{\theta_2}{C_{ox}^2}.Q_{iS}^2}{1 + \frac{\theta_1}{C_{ox}}.Q_{iD} + \frac{\theta_2}{C_{ox}^2}.Q_{iD}^2}\right) + \left(\frac{\theta_1}{\theta_2.n.kT/q} - 2\right) \times \ldots \\ \ldots \times \frac{C_{ox}^2}{\sqrt{\theta_1^2 - 4\theta_2}}.\left(atanh\left(\frac{\theta_1 + 2.\frac{\theta_2}{C_{ox}}.Q_{iS}}{\sqrt{\theta_1^2 - 4\theta_2}}\right) - atanh\left(\frac{\theta_1 + 2.\frac{\theta_2}{C_{ox}}.Q_{iD}}{\sqrt{\theta_1^2 - 4\theta_2}}\right)\right) \end{array}\right] \tag{12}$$

where Q_{iS} (resp. Q_{iD}) refers to the source (resp. drain) inversion charge.

Since in [8], all the MOSFET parameters have been extracted as a function temperature from 4.2K up to 300K for 28nm FDSOI MOS devices (as recalled in Fig. 6), the drain current model of Eq. (12) provides the drain current for any ambient temperature T using the interpolated values of V_t, n, μ_0, θ_1 and θ_2 as a function of temperature T.

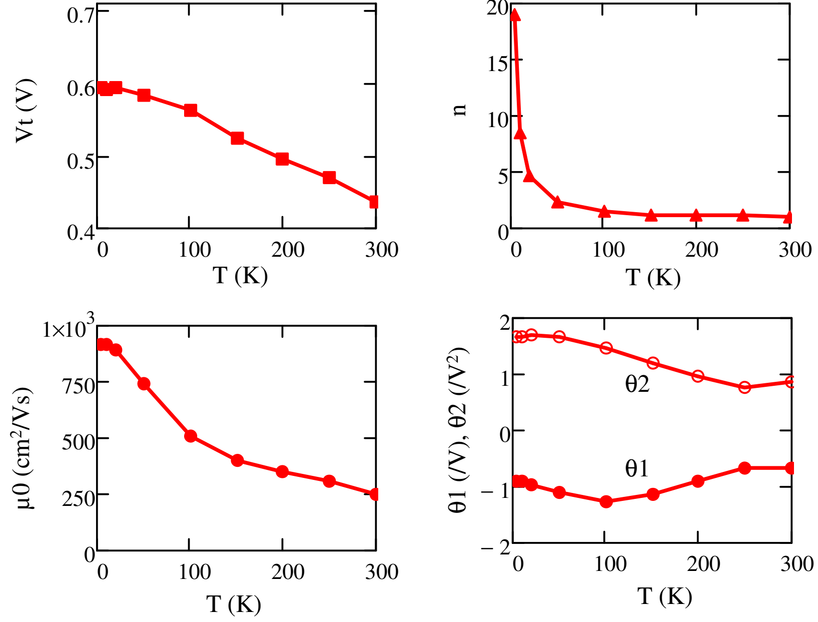


Fig. 6. Temperature dependence of the MOSFET parameters extracted for 28nm FDSOI devices used for drain current modelling (after [8]).

Therefore, this drain current model can be used to evaluate the impact of self-heating effect in such FDSOI devices thanks to the temperature rise model of Eq.(4). To this end, one should solve self consistently the equation relating the self-heated drain current I_{dSH}, with the drain current given by Eq. (12) in which the temperature is accounting for the power $I_{dSH}\times V_d$ through Eq. (4) such as,

$$I_{dSH} = I_d\left[V_g, V_d, T + \Delta T(I_{dSH} \times V_d, T)\right], \tag{13}$$

where the power P in $\Delta T(P,T)$ has been replaced by $I_{dSH}\times V_d$.

Typical results numerically obtained using Eqs (4), (12) and (13) and illustrating the impact of self-heating on the $I_d(V_d)$ output characteristics are shown in Fig. 7 for various ambiant temperatures. It is worth mentionning that the parameters A and T_0 of the differential thermal resistance used in Eq. (4) are those of the 28nm FDSOI technology with 25nm BOX thickness [5]. It should be noted that the larger impact of self-heating effect on the $I_d(V_d)$ curves with the onset of negative conductance, at lower ambiant temperature, is mainly due to the increasing thermal resistance at very low temperature. Indeed, as can be seen in Fig. 8, the device temperature T_{dev} (=ΔT +T) and temperature rise ΔT are significantly enhanced as the ambiant temperature is reduced. Note also that this increase strongly depends on the supply voltage used for the simulation.

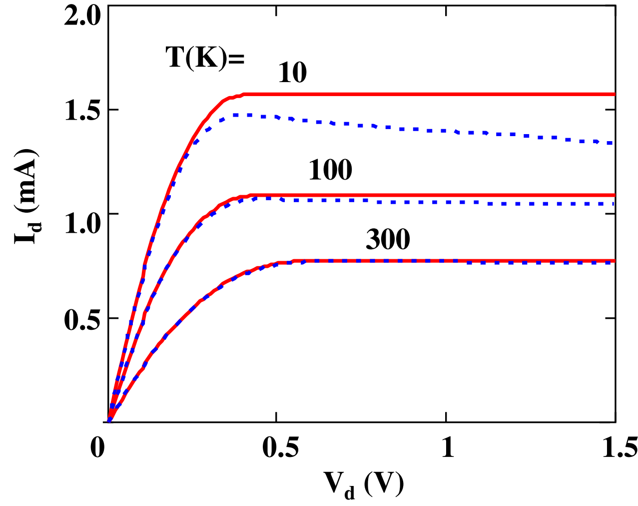


Fig. 7. $I_d(V_d)$ output characteristics as obtained from LW-function model without (solid lines) and with (dashed lines) self-heating effect for various ambient temperatures (T=10, 100 and 300K, V_g=1V, W=10µm, L=1µm, A=3.2×10^{4}K/W, T_0=60K, parameters of 28nm FDSOI MOSFETs with 25nm BOX thickness from [8]).

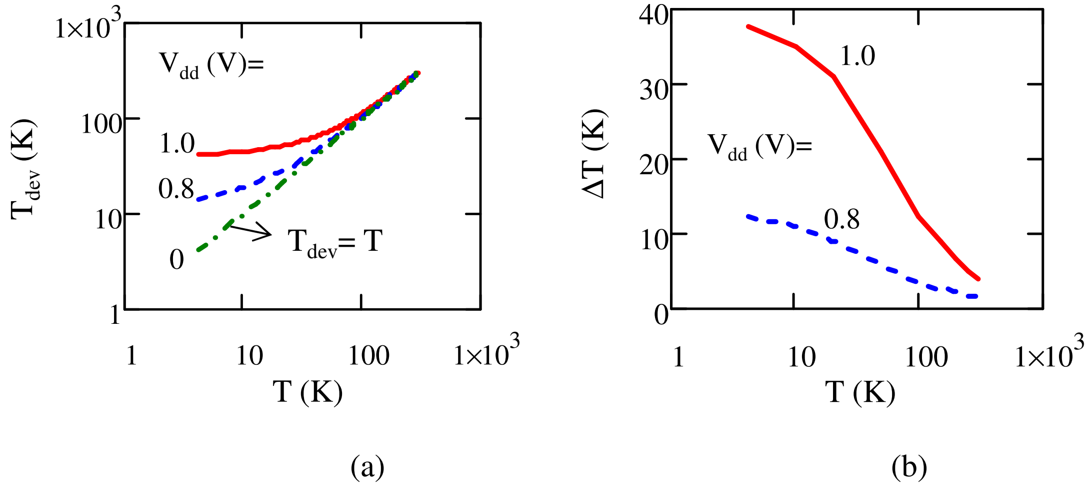
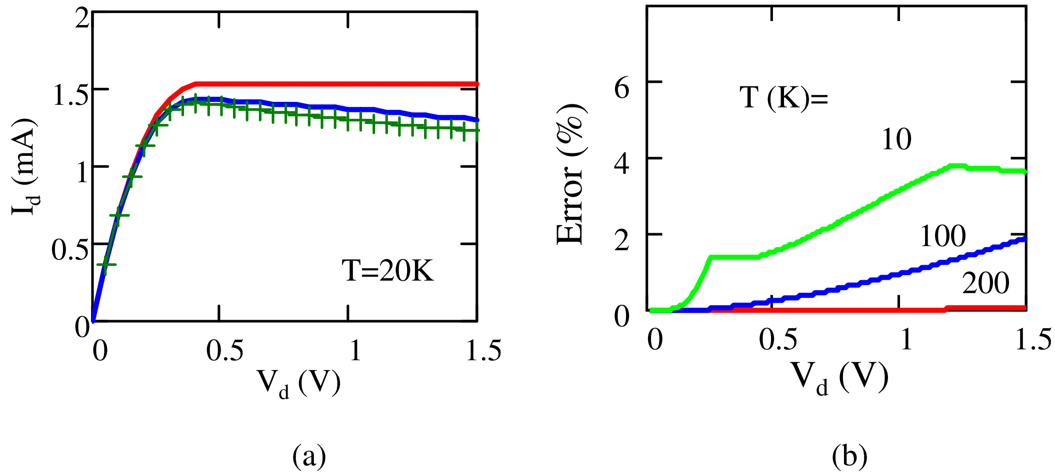


Fig. 8. Variations of device temperature T_{dev} (a) and self-heating temperature rise ΔT (b) with ambient temperature T for various supply voltage V_{dd}. (W=10µm, L=1µm, A=3.2×10^{4}W/K, T_0=60K, parameters of 28nm FDSOI MOSFETs from [8]).

Though very simple, the self-heating drain current model of Eq. (13) is not analytical and cannot be used as a compact model. Therefore, following the first order approach of [9, Eq. (9)], the self-heated drain current I_{dSH} can be approximated as,

$$I_{dSH}(V_g, V_d, T) = \frac{I_d(V_g,V_d,T)}{1-\frac{\delta \ln[I_d(V_g,V_d,T)]}{\delta T}.\Delta T[I_d(V_g,V_d,T)\times V_d,T]}. \quad (14)$$

Fig. 9(a) shows that this first order model does provide a good approximation for the self-heated drain current with an error found always smaller than ≈5% for ambient temperatures ranging from 4.2K to 300K, as illustrated in Fig. 9(b).



(a) (b)

Fig. 9. a) $I_d(V_d)$ output characteristics as obtained from numerical (blue solid line) and first order analytical (symbols) model with and without (red solid line) self-heating effect. b) Variations of percentage error vs V_d between numerical and first order analytical self-heating $I_d(V_d)$ models for various temperatures (V_g=1V, W=10μm, L=1μm, A=3.2×10^4W/K, T_0=60K, parameters of 28nm FDSOI MOSFETs from [8]).

4. Conclusion

We have performed a detailed analysis of the self-heating effect measured by gate thermometry in FDSOI MOSFETs operated at deep cryogenic conditions. We showed that the differential thermal conductance varies linearly with temperature over a wide range. Then we have provided for the first time an analytical formulation of the self-heating temperature rise ΔT as a function of power and ambient temperature in FDSOI and bulk MOSFETs valid down to very low temperatures. This self-heating temperature rise model has then been used to develop an original compact model for the self-heated drain current in FDSOI MOSFETs operated down to deep cryogenic temperatures. Finally, it is worth mentioning that this methodology could easily be extended to other kinds of device and technology.

Acknowledgments:

The authors would like to thank K. Triantopoulos for making available self-heating gate thermometry data obtained on FDSOI MOSFETs and already published in [5]. This work was partially supported by EU H2020 RIA project SEQUENCE under grant number 871764.

References

1. B. M. Tenbroek, M. S. L. Lee, W. Redman-white, R. J. T. Bunyan, and M. J. Uren, “Self - Heating Effects in SOI MOSFET’s and their measurement by small signal conductance techniques,” IEEE Transactions on Electron Devices, 43, 2240 (1996).
2. C. Xu, S. K. Kolluri, and K. Endo, “Analytical Thermal Model for Self-Heating in Advanced FinFET Devices With Implications for Design and Reliability,” IEEE Trans on Computer-Aided Design Int. Circ. Syst., 32, 1045 (2013).
3. C. Prasad, L. Jiang, D. Singh, M. Ag, J. Thomas, and P. Vandervoorn, “Self-heat Reliability Considerations on Intel’s 22nm Tri-Gate Technology,” in IEEE International Reliability Physics Symposium (IRPS), 2013, pp. 1–5.
4. C. Prasad, S. Ramey, and L. Jiang, “Self-heating in advanced CMOS technologies,” in IEEE International Reliability Physics Symposium (IRPS), 2017, pp. 6A–4.1–6A–4.7.
5. K. Triantopoulos, M. Casse, S. Barraud , S. Haendler, E. Vincent, M. Vinet, F. Gaillard, and G. Ghibaudo, “Self-Heating Effect in FDSOI Transistors Down to Cryogenic Operation at 4.2 K,” IEEE Transactions on Electron Devices, 66, 3498 (2019).
6. P. A. T Hart, M. Babaie, A. Vladimirescu, F. Sebastiano, “Characterization and Modeling of Self-Heating in Nanometer Bulk-CMOS at Cryogenic Temperatures”, IEEE Journal of the Electron De-vices Society, 9, 891 (2021).
7. T. A. Karatsori, C. G. Theodorou, E. G. Ioannidis, S. Haendler, E. Josse, C. A. Dimitriadis and G. Ghibaudo, "Full gate voltage range Lambert-function based methodology for FDSOI MOSFET parameter extraction", Solid State Electronics, 111, 123 (2015).
8. F. Serra di Santa Maria, L. Contamin, B. Cardoso Paz, M. Cassé, C. Theodorou, F. Balestra, G. Ghibaudo, “Lambert-W Function-based Parameter Extraction for FDSOI MOSFETs Down to Deep Cryogenic Temperatures”, Solid-State Electronics, 186, 108175 (2021).
9. J. Jomaah, G. Ghibaudo, F. Balestra, “Analysis and modelling of self-heating effects in thin film SOI MOSFETs as a function of temperature”, Solid State Electronics, 38, 615 (1995).