Scaling of GaSb/InAs Vertical Nanowire Esaki Diodes Down to Sub-10-nm Diameter

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***Abstract*—This work studies the diameter scaling behavior of broken-band GaSb/InAs vertical nanowire (VNW) Esaki diodes. A top-down fabrication process involving precise reactive-ion etching and alcohol-based digital etch has yielded devices with a tunneling junction diameter below 10 nm. Clear Esaki peaks are observed with an average peak current density of 1 MA/cm² and ideal areal scaling over two orders of magnitude in diameter. In the non-Esaki branch, an average current density of 4 MA/cm² is demonstrated at 0.3 V. This suggests a great potential for the broken-band GaSb/InAs system for ultra-low power VNW tunnel FET (TFET) applications. Towards evaluating the ultimate TFET potential of this material system, we have extracted the series resistance of our diodes and developed a model for it. We find that the main contribution to the series resistance comes from the GaSb body. Comparatively, the contact resistance at the top of the VNW has a minor impact in spite of the tiny Ni/InAs contact area. Self-consistent quantum transport simulations based on Non-Equilibrium Green's function formalism are carried out. We simulate two devices with different dimensions, i.e. one with strong quantum confinement and one with bulk-like behavior. Inelastic tunneling due to phonon emission is found to both widen the Esaki peak and to suppress tunneling in the non-Esaki branch.**

***Index Terms*—Esaki diode, Tunnel FETs, Nanowires, Top-down, III-Vs, GaSb, InAs, Digital etch, NEGF, Inelastic tunneling, Electron-phonon scattering, Contact resistance.**

I. Introduction

In the era of Internet of Things (IoTs), innovations in logic transistor technology that can achieve ultra-low power consumption and high performance are of great interest [1]. The fundamental limit of subthreshold swing (S) in MOSFETs prevents supply voltage (V_{dd}) scaling of Si CMOS technology, otherwise, the static power consumption in the off-state increases exponentially [2]. Transistors based on band-to-band tunneling (BTBT), usually referred to as tunnel FETs (TFETs), represent one of the most promising device designs capable of achieving a steep turn-on and therefore reduced power consumption [3].

Low BTBT current due to a wide tunneling barrier is one of the long-lasting problems in TFETs, which hampers their use in high-performance logic applications [4]. Considerable effort has been devoted to boosting BTBT current by careful tunnel junction design, from homojunctions composed of narrow-band materials [5], [6], to heterojunctions with staggered- and broken-band alignment [7], [8]. Among all possible designs, the GaSb/InAs material system offers the greatest potential, thanks to its broken-band alignment and excellent transport properties [9]. In spite of promising simulation results of GaSb/InAs TFETs [10], to date, experimentally demonstrated device performance, especially the drive current, has been disappointing [11]. Subthreshold swings (S) as low as 32 and 42 mV/dec over a small current range have been demonstrated in this material system by different research groups [12], [13]. However, on-state currents have remained well below what is desired [12], [13].

In order to exploit the high-quality GaSb/InAs heterojunction that can be grown through molecular-beam epitaxy (MBE) [14], a vertical device geometry is favored. For future logic nodes, a vertical nanowire (VNW) transistor design with sub-10-nm diameter is demanded [15], since it achieves small footprint and effective electrostatic charge control at the same time [16]. Recent experimental results on GaSb/InGaAsSb/InAs VNW TFETs have shown that an S as steep as 35 mV/dec could be maintained as the diameter was scaled down from 20 to 10 nm [17]. However, a ~30x degradation in BTBT current was also observed [17]. Strong quantization and thus a lower BTBT rate as diameter decreased were believed to be the reasons for this [17].

Towards contributing fundamental understanding behind this problem, we have fabricated and studied the scaling behavior of GaSb/InAs VNW Esaki diodes with a tunneling junction diameter down to 9 nm. To date, the smallest GaSb/InAs Esaki diodes that have been reported feature a diameter of 40 nm [18], [19], still far above the sub-10-nm scale of interest.

A preliminary report on our devices was given in [20]. This paper expands on that earlier presentation through a more detailed discussion on device fabrication process and current scaling behavior, as well as by developing a model for device series resistance. Furthermore, we carry out more accurate quantum transport simulations using the real dimensions of the fabricated devices. We also study the scaling of BTBT current by comparing a 11-nm diameter device with a bulk-like counterpart. Section II describes the device structure and process technology.

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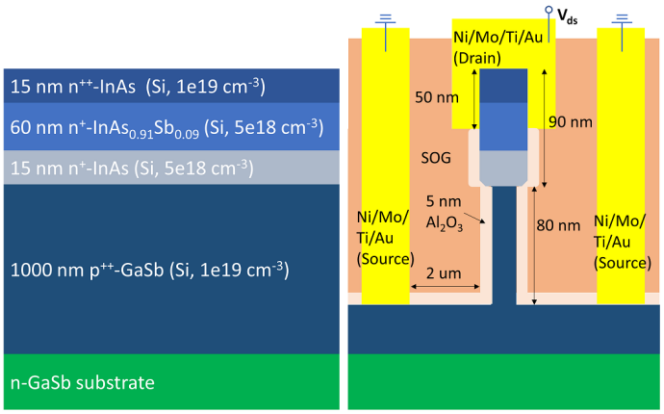

Fig. 1. Schematic cross-sectional diagrams of the starting heterostructure and the finished device.

Section III discusses device electrical characteristics and diameter scaling behavior. In Section IV, we formulate a series resistance model including mushroom top contact resistance, semiconductor resistance, and extrinsic non-scalable resistance. This model is validated by our experimental data. In section V, self-consistent Non-Equilibrium Green's functions (NEGF) simulations are carried out. The influence of inelastic electron-phonon scattering is quantitatively studied.

II. Device Fabrication

Fig. 1 shows schematic cross-sectional diagrams of the starting heterostructure grown by molecular beam epitaxy (MBE) and of a finished device. The heterostructure (described in detail in [20]) is fully-strained. This is expected to result in low defect density within the tunneling junction. We utilize Si as the only dopant throughout the entire heterostructure to achieve an abrupt doping profile at the tunnel junction, since Si is a p-type dopant in GaSb but an n-type dopant in InAs(Sb).

The device fabrication process flow is described in Fig. 2 (d), with schematic cross-sections and scanning electron microscope (SEM) pictures at key steps shown in Figs. 2 (a) to 2 (c). The process starts with electron-beam lithography (EBL) of a hydrogen silsesquioxane (HSQ) hardmask. VNWs are then dry etched using $Ar/BCl_3/SiCl_4$ chemistry in an inductively-coupled plasma (ICP) reactive-ion etching (RIE) etcher, following the recipe developed in [21]. A minimum diameter of 23 nm is obtained. Subsequently, 4 cycles of digital etch (DE) with pure oxygen and HCl:IPA are performed [22], [23]. Radial DE rates for GaSb and InAs(Sb) are ~1.7 and ~0.5 nm/cycle, respectively, due to different oxidation rates for the two materials. VNWs with GaSb diameter (D_{GaSb}) down to 9 nm are achieved, with the SEM of one of them shown in [20].

Immediately after DE, 5 nm Al_2O_3 is deposited by atomic layer deposition (ALD) for surface passivation. Device fabrication at this stage is illustrated in Fig. 2 (a) in a device with D_{GaSb} of 9 nm (9 + 2×5 = 19 nm). Spin-on-glass (SOG) is then applied to planarize the VNWs, followed by CF_4 RIE etch back to expose the HSQ mask on top. Al_2O_3 covering the HSQ mask is wet etched by TMAH. Fig. 2 (b) shows the schematic and SEM image at this stage. A second SOG layer is then applied and etched back (together with the HSQ hardmask) to expose the top of the VNWs and create an ohmic contact that extends along the sidewall. This is shown in Fig. 2 (c). Subsequently, a bottom contact via is opened by CF_4 RIE, followed by Al_2O_3 removal,

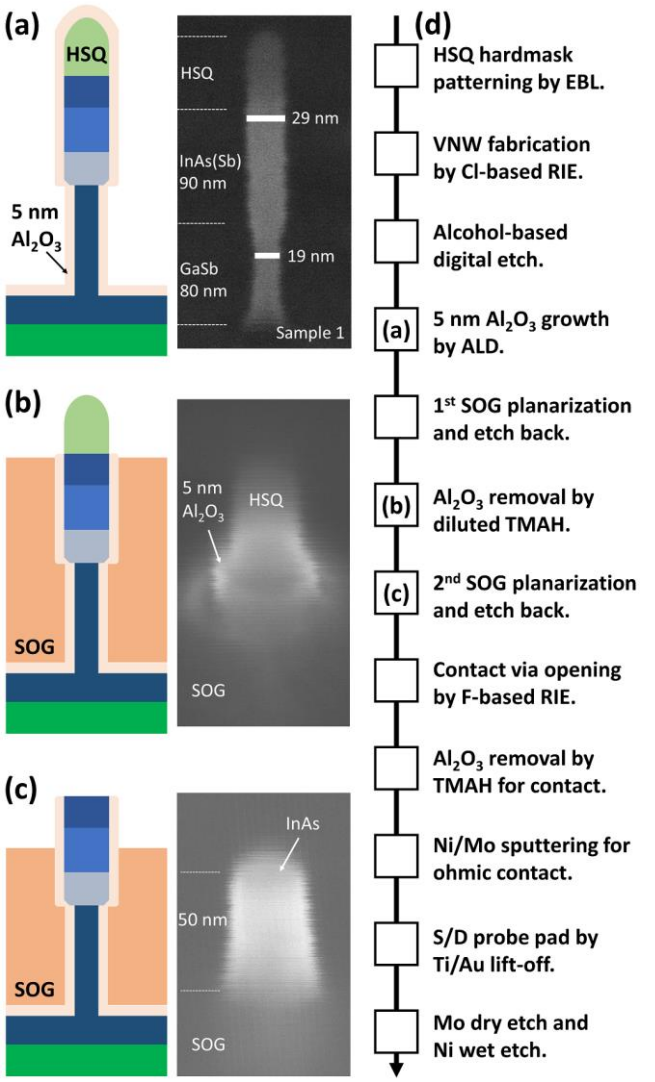

Fig. 2. Schematics of key processing steps and process flow. Schematics and corresponding SEM images after ALD Al_2O_3 growth (a); after 1st SOG planarization, etch back and Al_2O_3 removal (b); after 2nd SOG planarization and etch back (c). (d) Process flow for GaSb/InAs(Sb) VNW Esaki diode fabrication.

Ni/Mo sputtering, and Ti/Au pad lift-off. The device fabrication finishes by Mo dry etch with SF_6/O_2 RIE and Ni wet etch with Ni etchant using the pads as mask.

The final devices feature single VNWs with D_{GaSb} ranging from 9 nm to 1000 nm. Two samples (samples 1 and 2) are fabricated at different times through an identical process except that more DE cycles are applied on the latter one. The smallest D_{GaSb} achieved in sample 2 is 10 nm.

III. Electrical Characteristics and Diameter Scaling

We use a TFET-like voltage sign convention (V_{ds}) such that a positive V_{ds} refers to the reverse regime of the p-n junction (n-region positive with respect to p-region). All current density values are calculated with respect to the cross-sectional area of GaSb since that is the narrowest location of the tunnel junction.

Fig. 3 (a) shows *I-V* characteristics of an exemplar D_{GaSb} = 11 nm device in log scale. This device exhibits clear negative differential resistance (NDR) with a peak current density (J_{peak}) of 2.3 MA/cm^2 and a peak-to-valley current ratio (PVCR) of 2.1

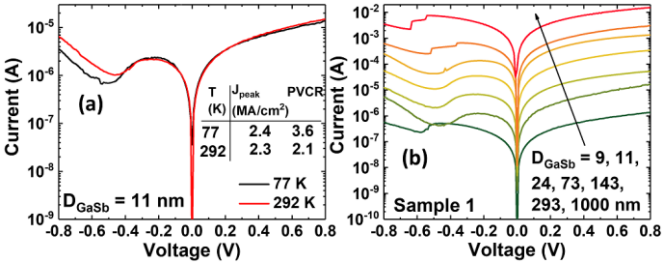

Fig. 3. (a) *I-V* characteristics of a D_{GaSb} = 11 nm device from sample 1 measured at RT and 77 K. Figures of merit are listed in the inset. (b) *I-V* characteristics at RT for devices from sample 1 with different diameters.

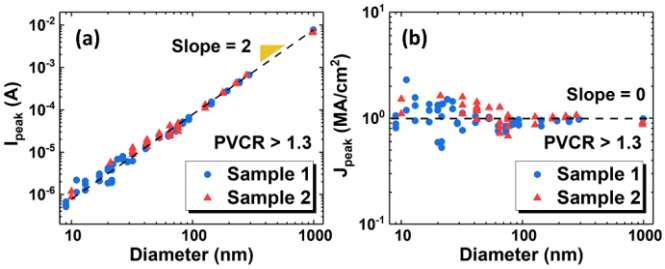

Fig. 4. Diameter scaling of peak current (a) and peak current density (b) of devices with PVCR > 1.3 from samples 1 and 2.

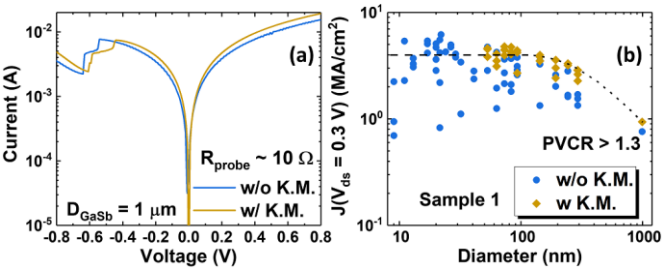

Fig. 5. (a) *I-V* characteristics of a D_{GaSb} = 1 μm device from sample 1 with and without Kelvin measurement (K.M.). (b) Diameter scaling of current density at 0.3 V of devices with PVCR > 1.3 from sample 1.

at room temperature (RT). PVCR is found to increase to 3.6 at 77 K with J_{peak} unchanged, suggesting the suppression of trap-assisted tunneling (TAT) at the Esaki valley [24]. For voltages larger than the Esaki peak voltage ($|V_{peak}|$, the absolute value of V_{ds} at which the peak current occurs), we observe temperature-independent characteristics suggesting that pure BTBT is the dominant current mechanism.

Fig. 3 (b) shows *I-V* characteristics of devices with different diameters, from 9 to 1000 nm, at RT. $|V_{peak}|$ is independent of diameter except for the narrowest and the widest devices, which both suffer from series resistance (discussed in Sec. IV). In the narrowest device, the excess resistance arises from a non-optimal top contact [20]. For the widest device, it is due to an extrinsic non-scalable resistance that might come from the aggregate of bottom contact, probe pads and probe tips, all estimated to be ~30 Ω, as we will discuss below.

Our Esaki diodes display near-ideal diameter scaling behavior. This is illustrated in Fig. 4 that shows the evolution of Esaki peak current (I_{peak}) and peak current density, J_{peak}, as a function of tunneling junction diameter. We choose devices that exhibit PVCR > 1.3 since I_{peak} of these devices are minimally affected by the excess valley current. A clear quadratic relationship between I_{peak} and D_{GaSb} is demonstrated on these devices over the entire diameter range. An average J_{peak} = 1 MA/cm² is achieved. I_{peak} scaling in both samples 1 and 2 is identical. This is in spite of the fact that VNWs from both samples have a similar D_{GaSb} of 9 and 10 nm but quite different D_{InAs} of 19 and 35 nm, respectively (an SEM image of a VNW from sample 2 can be found in [20]). The consistent values of J_{peak} across both samples confirm that BTBT is limited by the GaSb side of the junction.

Of greater relevance for ultra-low power GaSb/InAs VNW TFETs is the positive V_{ds} current branch of our Esaki diodes. In Fig. 3 (a) we observe that it is temperature-independent, consistent with pure BTBT. To quantify our results, we graph in Fig. 5 (b) the current density at V_{ds} = 0.3 V (denoted as $J(V_{ds}$ = 0.3 V)), as this is the target operating voltage for a future TFET technology [10]. To minimize the impact of non-scalable extrinsic resistance due to probing (R_{probe}), in wide diameter devices we carry out Kelvin measurements. Fig. 5 (a) shows a D_{GaSb} = 1 μm device with and without Kelvin probing. From the decrease of $|V_{peak}|$ after performing the Kelvin measurement and the value of I_{peak}, we calculate R_{probe} ~ 10 Ω, which is within the 30 Ω non-scalable resistance mentioned above. As shown in Fig. 5 (b), ideal scaling of $J(V_{ds}$ = 0.3 V) is observed across most of the diameter range, with an average value of 4 MA/cm² demonstrated. For large-diameter devices, the current level is also large and the voltage drop on the extrinsic resistance becomes significant even in a Kelvin configuration. We estimate a similar value of the resistance base on the $J(V_{ds}$ = 0.3 V) drop on large-diameter devices.

IV. Series Resistance Measurements and Model

The series resistance, R_s, plays a key role in limiting the current of VNW devices. Towards evaluating this, we have extracted R_s of our diodes from their forward *I-V* characteristics passed the Esaki peak ($|V_{ds}| > |V_{peak}|$). We can derive R_s starting from the *I-V* characteristics of a p-n junction in the forward regime at a $|V_{ds}|$ greater than several k_BT/q [25]:

$$I \approx I_s \exp\frac{q(|V_{ds}| - IR_s)}{nk_BT} \quad (1)$$

where I_s is the saturation current, n is the ideality factor, and the rest of the symbols have their usual meanings. From (1) and after some straightforward math, we derive a simple expression for the differential resistance, r:

$$r = \frac{d|V_{ds}|}{dI} = R_s + \frac{nk_BT}{qI} \quad (2)$$

Equation (2) suggests a direct way to estimate R_s in our devices: a linear regression of r *versus* k_BT/qI on the high negative V_{ds} regime where the carrier transport can be described by (1). We obtain good fittings on almost all devices if we choose the fitting range to start from $|V_{ds}|$ = 0.7 V till the highest value that we measure (typically 0.8 V). R_s in large-diameter devices is generally limited by extrinsic resistance, as noted above. In these cases, the fittings are performed at higher $|V_{ds}|$ values. An example of the R_s extraction process is shown in the inset of Fig. 6 for a 143-nm diameter device. The *I-V* characteristics of the same device are also shown. Using the above procedures, we extract R_s *versus* D_{GaSb} data with and without Kelvin probing, with the results shown in Fig. 7 (b) (dots), where a scaling behavior of $R_s \propto D_{GaSb}^{-2}$ is observed on all devices except for the larger diameter ones.

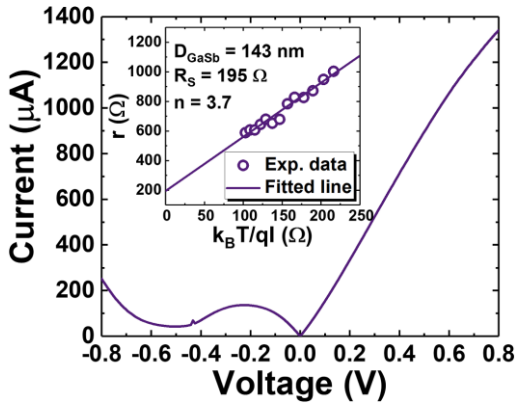

Fig. 6. *I-V* characteristics of a D_{GaSb} = 143 nm device. Inset shows the linear regression between differential resistance and k_BT/ql, through which series resistance and ideality factor are extracted.

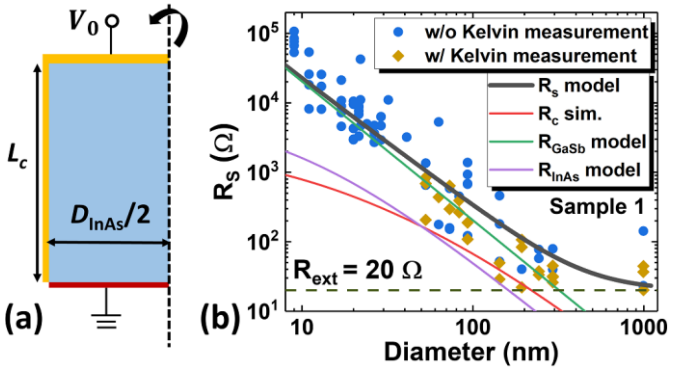

Fig. 7. (a) Radial cross section of the Ni/n^{++}-InAs top contact for R_c TCAD simulations. Yellow and red edges denote the top contact, with an applied voltage of V_0, and ground, respectively. (b) R_s *versus* GaSb diameter for extracted R_s from experimental results from sample 1 (dots) and for modeled R_s (black line). Different components of R_s including R_c, R_{GaSb}, R_{InAs}, and R_{ext} are also shown.

We have constructed a model for the series resistance of our devices. To the first order, this can be expressed as:

$$R_s = R_c + R_{\mathrm{InAs}} + R_{\mathrm{GaSb}} + R_{\mathrm{ext}} \quad (3)$$

Here, $R_{\mathrm{InAs}} = 4\rho_{\mathrm{InAs}}(L_{\mathrm{InAs}} - L)/\pi {D_{\mathrm{InAs}}}^2$ is the longitudinal resistance of the uncontacted portion of the n$^+$-InAs(Sb) region, $R_{\mathrm{GaSb}} = 4\rho_{\mathrm{GaSb}}L_{\mathrm{GaSb}}/\pi {D_{\mathrm{GaSb}}}^2$ is the longitudinal resistance of the p$^+$-GaSb region, R_c is the n^{++}-InAs/Ni top contact resistance, and $R_{\mathrm{ext}} = 20\ \Omega$ is the non-scalable resistance (excluding the contact resistance between probe pad and probe tips that can be corrected by Kelvin measurement as shown in Fig. 5 (a)). The bottom contact resistance to p$^+$-GaSb is small since the contact area is very large. In addition, this resistance is the same for all the devices we fabricate, so it is part of R_{ext}.

To calculate R_c, we carry out simulations in *Synopsys* TCAD *Sentaurus* simulator, in which Poisson equation is solved. A 2D cylindrical coordinate system enables efficient simulations of our radially symmetric 3D structure. The simulation geometry (radial cross section) is shown in Fig. 7 (a), where a NW is contacted from the sidewall (with a length of L_c), as well as from the top surface. We extract R_c for different InAs diameter structures from the slope of the simulated *I-V* characteristics.

Using (3) and the materials and device parameters of Table I, we can predict R_s *versus* D_{GaSb}. The specific contact resistance (ρ_c) for the Ni/n^{++}-InAs ohmic contact is adopted from [26] at $N_D = 10^{19}$ cm^{-3}, ρ_{GaSb} is calculated using the formula given in

TABLE I
PARAMETERS FOR SERIES RESISTANCE MODELLING

ρ_c (Ω.cm^2)	ρ_{InAs} (Ω.cm)	ρ_{GaSb} (Ω.cm)	L_{InAs} (nm)	L_{GaSb} (nm)	L_c (nm)
10^{-8}	7×10^{-4}	2×10^{-3}	90	80	25

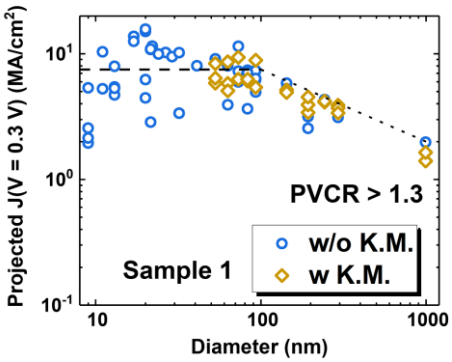

Fig. 8. Projected intrinsic BTBT current at V = 0.3 V *versus* GaSb diameter for sample 1 after correcting for series resistance. Only devices with PVCR > 1.3 are included. K.M. refers to Kelvin measurements.

[27] at a doping level $N_A = 10^{19}$ cm^{-3}, and ρ_{InAs} is adopted from [28] at a doping level $N_D \approx 6\times10^{18}$ cm^{-3}, which is similar to the nominal doping level of the n$^+$-InAs(Sb) portion of our devices. We adopt L_c = 25 nm since Al_2O_3 is removed only from the top 25 nm of the VNW, as observed in an SEM measurement right before contact metal sputtering.

Fig. 7 (b) shows the modeled R_s (black line) from (3) as a function of D_{GaSb}. Excellent agreement is obtained with the experiments, verifying the validity of the assumptions behind our model. If we look at the components of R_s, R_{GaSb} (green line) is found to contribute the most, over most of the diameter range, while the contribution of R_c (red line) is insignificant in all cases. This model explains the observed scaling behavior of $R_s \propto {D_{GaSb}}^{-2}$ on sub-200-nm diameter devices. This is further indication of the near-ideal nature of our devices. Our model also suggests that R_{InAs} (purple line) is around one order of magnitude smaller than R_{GaSb}. This is understandable since the InAs portion of our diodes has a larger diameter and a higher majority carrier mobility than the GaSb portion. R_s of large diameter devices eventually saturates at 20 Ω, the value of the extrinsic resistance. Interestingly, R_s of the D_{GaSb} = 9 nm devices somehow deviates from the model, which might result from a non-ideal top contact as discussed in Section III. An increased ρ_c value of 4×10^{-7} Ω.cm^2 could explain this observation.

Knowing R_s allows us to project the intrinsic BTBT current density at V = 0.3 V by subtracting the voltage drop on the extracted R_s. This is of relevance for TFET operation of this layer structure. An average projected $J(V = 0.3\ \mathrm{V})$ of 7.5 MA/cm^2 is obtained for sub-100-nm diameter devices, as shown in Fig. 8. As expected, we do not see any difference with or without Kelvin probing. A degraded current density is found for wider devices. A possible reason for this is that there might be some residual resistance that we do not fully correct for. Interestingly, detailed simulations (Section V) for different device diameters also suggest this behavior. Nevertheless, this exercise shows the great potential for high drive current of scaled GaSb/InAs VNW TFETs with optimized geometry.

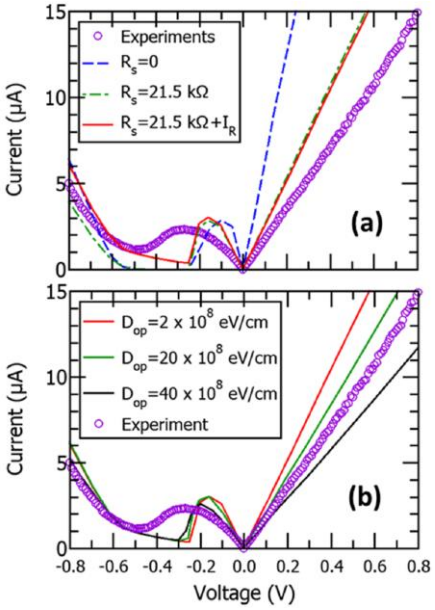

Fig. 9. Simulated (lines) and experimental (symbols) *I-V* curves for the D_{GaSb} = 11 nm device. (a) Simulations with and without experimentally estimated R_s and fitted I_R. (b) Simulations including R_s, I_R as in (a) and inelastic polar optical phonon scattering for different deformation potential (D_{op}) values.

V. Quantum Transport Simulations

In order to support the interpretation of our experiments, we have performed self-consistent simulations within the Non-Equilibrium Green's functions (NEGF) formalism and adopt an 8×8 k·p Hamiltonian to describe the materials properties [29]. Heterojunctions are described in the real-space Hamiltonian by means of position-dependent k·p parameters [30], and particularly by using the material parameters given in [31]. Tensile strain in the InAs and InAsSb layers induced by lattice mismatch with GaSb is accounted for by employing the strain interaction matrix discussed in [29], and with deformation potentials from [31]. Band gap narrowing due to the high doping concentrations in GaSb and InAs(Sb) is also included according to the experimental values reported in [32], [33].

The simulated devices have a length of the GaSb, InAs, and InAsSb regions equal to the features of the measured samples sketched in Fig.1 (see also the *x*-axis in Figs.10 and 11, where the direction of *x*-axis is the longitudinal transport direction). The numerical burden implied by 3D quantum simulations of such relatively long and wide device structures has been softened by adopting the coupled mode-space approach [31], [34]. We typically use 50 modes for the valence band (VB) of GaSb and 30 modes for the conduction band (CB) of InAs(Sb). Inelastic phonon scattering is also included by using a local formulation for the phonon self-energies, and within the self-consistent Born approximation [34]. We treat acoustic phonons in the elastic approximation, and polar phonons as dispersion-less optical phonons with a phonon energy $\hbar\omega$ = 30 meV.

Figure 9 (a) compares the simulated (lines) and measured (symbols) *I-V* characteristics of a device with D_{GaSb} = 11 nm and D_{InAs} = 21 nm, where simulations do not account for phonon scattering. The agreement with experiments is improved both at positive and negative V_{ds} regimes by including the influence of a series resistance R_s = 21.5 kΩ, whose value is inferred from Fig. 7 (b) for a GaSb diameter of 11 nm. The simulated valley current tends to largely underestimate experiments, which may be due to the fact that simulations do not include any TAT mechanism [24]. In Fig. 9, we have tried to improve this aspect by introducing a simple, phenomenological model for a non-ideal recombination current, which has the form $I_R = I_{R0}\left[\exp\left[\frac{q|V_{ds}|}{n_R k_B T}\right] - 1\right]$ in the space charge region, where the pre-factor I_{R0} has been adjusted to approximately reproduce the Esaki valley current. Still the simulations in Fig. 9 (a) exhibit, compared to experiments, a larger current for positive V_{ds} regime and a narrower NDR region with a lower $|V_{peak}|$.

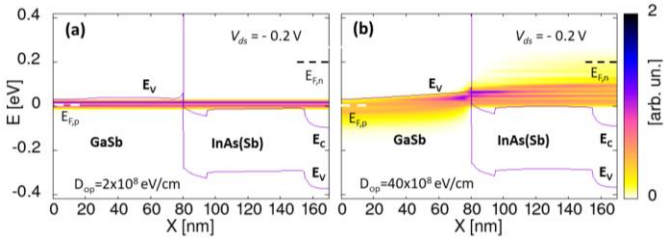

Fig. 10. Current spectra for the simulations in Fig. 9 (b) at V_{ds} = -0.2 V. (a): D_{op} = 2×10^8 eV/cm and (b): D_{op} = 40×10^8 eV/cm. The energy reference is the Fermi level ($E_{f,p}$) in GaSb, so that $E_{f,n}$ on the InAs side is given by -qV_{ds}. The lines refer to the spatial profiles of the highest valence subband (E_v) and of the lowest conduction subband (E_c).

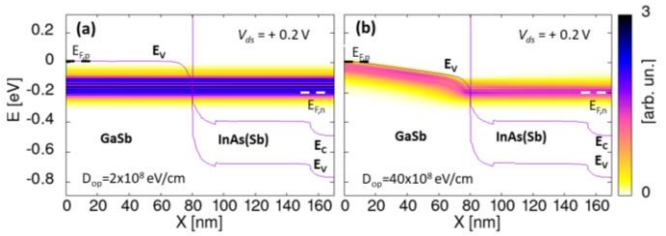

Fig. 11. Current spectra as in Fig. 10 but here for V_{ds} = +0.2 V.

Fig. 9 (b) shows that the inclusion of phonon scattering improves both aspects above. In fact, Fig. 10 shows that for V_{ds} = -0.2 V, phonon emission opens an inelastic tunneling path at the tunneling junction located approximately at x = 80 nm, which tends to push $|V_{peak}|$ higher in the NDR region. For V_{ds} = +0.2 V, instead, Fig. 11 reveals that phonons essentially act as a diffusive scattering mechanism that degrades BTBT current. This is particularly clear in the narrower and therefore more resistive quasi-neutral GaSb region, where the resistive voltage drop is not negligible. In both Fig. 10 and Fig. 11 the effect of phonons is much weaker in plots (a) compared to plots (b), because of the corresponding smaller deformation potential, D_{op}.

The last simulation-based analysis is devoted to a better understanding of the diameter scaling behavior of J_{peak}, as shown in Fig. 4. In order to approximate a bulk-like device by using our numerical simulation approach, we have used a large diameter and then employed periodic boundary conditions for the discretization of the 8×8 k·p Hamiltonian at the perimeter of the simulation domain according to the method presented in [35]. We have verified that periodic boundary conditions ensure that the current per unit area in the device is independent of the actual diameter used in simulations when the diameter is larger than ~20 nm. Such periodic boundary conditions effectively suppress any size-induced quantization effects. A sizeable bandgap widening in GaSb region is instead observed in the

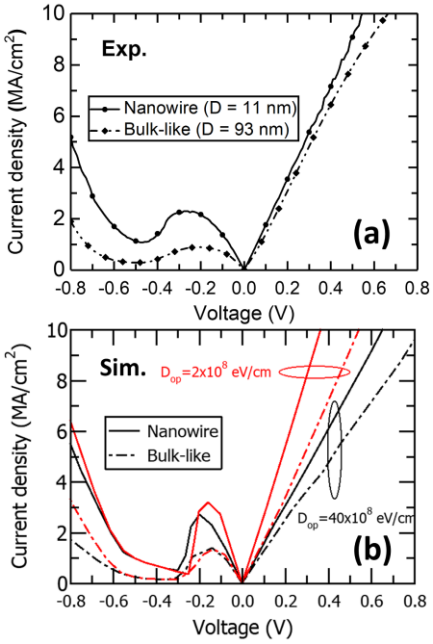

Fig. 12. *J-V* characteristics of experimental results (a) and simulation results (b) for a D_{GaSb} = 11 nm device and a bulk-like device. Current density is normalized with respect to the cross-sectional area of GaSb. Two values of deformation potential are compared in the simulations for both devices.

D_{GaSb} = 11 nm NW (not shown), where closed boundary conditions have been employed at the perimeter of the device cross section.

In Fig. 12, simulations confirm the experimental observation that the current density in the D_{GaSb} = 11 nm device does not degrade with respect to large diameter devices, but actually is enhanced. Within the inevitable scattering in the measured J_{peak} values reported in Fig. 4 (b), a larger average J_{peak} in narrow nanowires (compared to bulk-like devices) is also observed even in experiments for diameters between 10 and 20 nm. Hence both experiments and simulations suggest that size-induced quantization does not induce a degradation of the current density in the VNW GaSb/InAs Esaki diodes studied in this work.

VI. Discussion

A detailed benchmarking of our devices against the state-of-the-art can be found in [20]. Our devices achieve the best performance at our nominal doping level with a diameter that is reduced by a factor of >4 below that of any prior device.

In order to understand the excellent results demonstrated in this work, we summarize the following five criteria for designing and fabricating GaSb/InAs Esaki diodes with high BTBT current. These arguments also apply to the design of TFETs in this materials system.

(1) High doping level, especially in the p-GaSb region. High doping levels enhance BTBT due to shorter tunneling paths and more available states to tunnel from and to tunnel into. The valence band effective density of states (N_v) of GaSb has a value of 1.8×10^{19} cm^{-3} [31], which is much larger than the conduction band effective density of states (N_c) of InAs with a value of 8.7×10^{16} cm^{-3} [31]. To achieve degenerate doping in p-GaSb, a doping level on the order of 10^{19} cm^{-3} is needed. On the other hand, the doping level in n-InAs is not as critical. In our work, we choose a value of 5×10^{18} cm^{-3}. A way to compare the tunneling performance of different devices with different combinations of doping levels is to define an effective doping level, $N_{eff} = N_A N_D/(N_A+N_D)$, based on N_A in p-GaSb region and N_D in n-InAs region. When done in this way, for equivalent N_{eff}, our devices perform as good as the best in the literature [20].

(2) Abrupt composition transition from GaSb to InAs enabled by MBE. This is critical for achieving a desired band alignment, in our case, a broken-band configuration. If the transition is graded, as is the case in MOCVD grown structures, the band alignment becomes staggered-band, and the tunneling path gets significantly longer. To date, only MBE growth can achieve an abruptness within several atomic layers and a high tunneling rate, as demonstrated in the literature [20].

(3) Abrupt doping type transition from p-GaSb to n-InAs enabled by Si doping. This is also to minimize doping gradients and shorten the tunneling path. Even with the commonly-used *in-situ* doping during MBE growth, the doping gradient at the junction can be on the order of 5 nm/dec. Therefore, using Si on both sides of the tunneling junction minimizes the grading of the transition to within a few atomic layers.

(4) Lattice-matched substrate and heterojunction. A heterostructure closely lattice-matched to the substrate can be fully strained and therefore include a minimum density of threading dislocations that might originate from epitaxy layer relaxation. Low interface trap density at the junction is key to large PVCR of an Esaki diode, due to low TAT rate. In our design, by including Sb into n^+-InAs layer, a lattice constant identical to that of GaSb can be maintained, making the heterostructure fully strained [36].

(5) Critical dimension smaller than 100 nm. As we have shown, a device with a diameter larger than 100 nm suffers from extrinsic resistance that limits its performance at positive V_{ds} regime. As a result, scaling down the device dimension is highly favorable.

VII. Conclusions

We present a detailed study of scaling behavior of VNW GaSb/InAs Esaki diodes. These devices exhibit ideal current scaling over two orders of magnitude of diameter, from sub-10 nm to 1 µm. We model the total series resistance in our devices based on merely material- and device-related parameters and find that it is dominated by the resistance of the GaSb portion of the diode. Quantum transport simulations show that device characteristics, especially the positive V_{ds} branch, can be reproduced by adding the inelastic electron-phonon scattering mechanism. Our results clearly demonstrate a high drive current potential of ultra-scaled VNW GaSb/InAs TFETs for future VLSI applications. They also suggest several reasons for the long-lasting mismatch between III-V TFET modeling and experimental demonstrations.

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