Improvement of the electrical performance of Au/Ti/HfO 2 /Ge 0.9 Sn 0.1 p-MOS capacitors by using interfacial layers

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ABSTRACT

The impact of different interfacial layers (ILs) on the electrical performances of Au/Ti/HfO_2/$Ge_{0.9}Sn_{0.1}$ metal oxide semiconductor (MOS) capacitors is studied. Parallel angle resolved x-ray photoelectron spectroscopy measurements show that germanium diffuses into the HfO_2 layer when no IL is used. This results in an increase in the tin content at the interface and a high interface state density. We demonstrate that the use of an IL prevents germanium and HfO_2 intermixing and improves the electrical performance of MOS capacitors. Several ILs are studied such as alumina (Al_2O_3) and plasma oxidized GeSn ($GeSnO_x$) prior to HfO_2 deposition. C–V measurements correlated with simulations made by a customized analytical model indicate an interface state density of 5×10^{11} eV^{-1} cm^{-2} for the HfO_2/$GeSnO_x$/$Ge_{0.9}Sn_{0.1}$ gate stack. This result is promising for the integration of high mobility GeSn channels in CMOS devices.

The introduction of materials with carrier mobilities higher than silicon (Si) is important to further improve the performance of metal oxide semiconductor field effect transistors (MOSFETs). In this respect, the germanium tin (GeSn) alloy is a very promising candidate since it exhibits a direct and low bandgap for Sn contents >7.1%,[1] has high carrier mobilities,[2,3] and belongs to group-IV semiconductors. These assets make it interesting for its introduction as a channel material into pFET transistors. Recently, several research groups reported on the growth of high-quality GeSn epitaxial layers on Si wafers by means of chemical vapor deposition (CVD)[4–7] and molecular beam epitaxy (MBE).[8,9] This breakthrough enables development of devices such as high ON-current MOSFETs,[10–14] Schottky-barrier FETs (SBFETs), or tunnel FETs (TFETs).[15–18] However, the device performance does not depend only on the material properties of the channel, but also on the electrostatic control of the gate. Hence, the fabrication of high-k/GeSn gate stacks with a good interfacial quality is key to obtaining high performance GeSn-based devices.

Atomic layer deposition (ALD) is the most suitable technique for the deposition of high-k materials such as Al_2O_3, HfO_2, and ZrO_2 at a low temperature ($\leq$250 °C) with excellent uniformity and well controlled thicknesses. Nevertheless, this deposition process results in a high surface state density (D_{it}), degrading the electrical performance of pMOS capacitors. For this, wet chemical treatments and/or the addition of an interfacial layer (IL)[19] were proposed prior to the high-*k* deposition in order to reduce the D_{it} and enhance the reliability of the manufactured devices. Several studies, such as those of Gupta *et al.*,[14] Han *et al.*,[16] and Mahjoub *et al.*,[20] focused on the impact of wet cleaning on devices. Meanwhile, Wirths *et al.*[21] evaluated the interface quality for different high-*k* stacks on GeSn and strained Ge. However, that study focused mainly on strained Ge with an incomplete investigation of high-*k*/GeSn stacks.

In this work, we report on the fabrication of various $Ge_{0.9}Sn_{0.1}$ based p-type MOS capacitors with different dielectric stacks. These structures will be investigated in order to determine which dielectric stack yields the best interface with the $Ge_{0.9}Sn_{0.1}$ channel. High-resolution transmission electron microscopy (HR-TEM) is used to evaluate the morphology and quality of the dielectric/GeSn stacks. Capacitance–voltage (C–V) measurements together with theoretical calculations are performed to extract the D_{it} for each p-type MOS capacitor. Finally, parallel angle-resolved X-ray photoelectron spectroscopy (pAR-XPS) is used to investigate the physical and chemical

properties of the dielectric/GeSn interfaces in relation to their electrical characteristics.

The 50 nm thick $Ge_{0.9}Sn_{0.1}$ layer used in this work was grown on a 2.5 μm thick Ge strain relaxed buffer (Ge SRB) grown itself on an Si (100) substrate in a 200 mm Epi Centura 5200 reduced pressure chemical vapor deposition (RP-CVD) cluster tool from Applied Materials. Further details can be found elsewhere.[22] The high-k layers were deposited at 250 °C in a Fiji–Savannah (ALD) tool. Trimethylaluminium (TMA, Epichem, 99.9%), tetrakis(dimethyllamido)hafnium (TDMAH), and de-ionized water (Di-H_2O, Epichem, 99.9%), were used as the aluminum, hafnium, and oxygen precursors, respectively. $GeSnO_x$ was formed with an *in situ* oxygen plasma prior to the high-k deposition. After high-k dielectric deposition, 5 nm of titanium and 145 nm of gold were evaporated in a MEB550 tool from PLASSYS in order to form the MOS structures with conventional photolithography and liftoff steps.

In this work, four samples were fabricated with different dielectric stacks. Prior to this process, all samples underwent the same wet chemical treatment which consisted of a surface degrease, a dip in HF for 1 min, and a dip in $(NH_4)_2S$ for 30 min.[20] The dielectric stacks of the four samples are detailed in Table I.

XPS and pAR-XPS analysis were performed on a customized Thermo Fisher Scientific Theta 300 system with ultrahigh vacuum conditions ($<1\times10^{-8}$ Pa) equipped with an X-ray source using a monochromatic aluminum anode (1486.6 eV). The analyzer has a two-dimensional detector, allowing parallel acquisition at eight emission angular ranges of 7.5° from 20° to 80° without any tilt of the sample. HR-TEM imaging was performed on a TEM TECNAI from Thermo Fisher Scientific with an incident electron beam of 200 keV. For the HRTEM observation, a thin lamella of the MOS structure was prepared by using a Helios NanoLab 450s FIB-SEM tool from FEI (Fisher Scientific), combining a Ga^+ focused ion beam and an electron beam. C–V measurements were carried out with a Keithley 4200A SCS analyzer.

Figure 1 shows the cross-sectional HRTEM images of samples S1, S2, S3, and S4. The different dielectric layers deposited on the crystalline GeSn layer are clearly seen. The experimental thickness of each layer is in a good agreement with the expected one. In addition, a certain roughness at the GeSn/dielectric interface can be observed for all samples. It could be due to the initial surface roughness of the as-grown GeSn layer [the surface root mean square (rms) roughness is indeed equal to 0.43 nm for the 5×5 μm^2 AFM images[6]].

Capacitance–voltage measurements were carried out in order to evaluate the impact of the different dielectric stacks on the electrical properties of the MOS capacitors.

To suppress the contribution of the series resistance to the C–V curves, a correction of the measured capacitance (C_m) has been applied using the following formula:[22]

TABLE I. Description of the samples investigated in this work.

Sample name	Description of the gate stacks
S1	GeSn/1 nm-$GeSnO_x$/1 nm-Al_2O_3/7 nm-HfO_2
S2	GeSn/1 nm-Al_2O_3/9 nm-HfO_2
S3	GeSn/1 nm-$GeSnO_x$/8 nm-HfO_2
S4	GeSn/9 nm-HfO_2

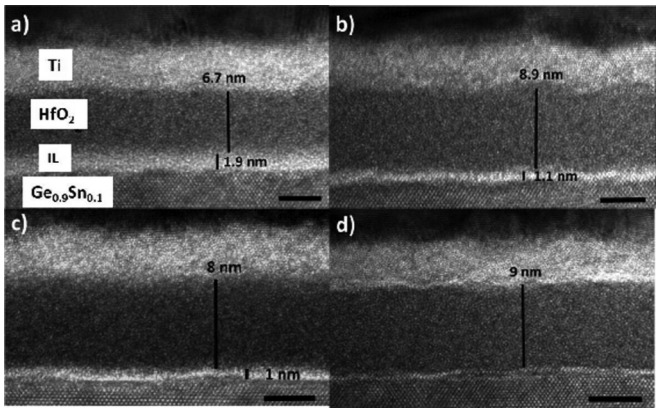

FIG. 1. Cross-sectional HR-TEM images of (a) S1, 1 nm-$GeSnO_x$/1 nm-Al_2O_3/7 nm-HfO_2, (b) S2, 1 nm-Al_2O_3/9 nm-HfO_2, (c) S3, 1 nm-$GeSnO_x$/8 nm-HfO_2, and (d) S4, 9 nm-HfO_2 gate stacks. The scale bars are 5 nm for all images.

$$C_c = \frac{\left(G_m^2 + \omega^2 C_m^2\right) C_m}{a^2 + \omega^2 C_m^2}, \tag{1}$$

where C_c, C_m, and G_m are the corrected capacitance, the measured capacitance, and the measured conductance, respectively, and $\omega = 2\pi f$

$$a = G_m - \left(G_m^2 + \omega^2 C_m^2\right) R_s \tag{2}$$

with

$$R_s = \frac{G_{ma}}{G_{ma}^2 + \omega^2 C_{ma}^2}, \tag{3}$$

where G_{ma} and C_{ma} are the conductance and the capacitance measured in strong accumulation, respectively.

Figures 2(a) and 2(b) show the normalized C–V characteristics for all samples at 6 and 200 kHz, respectively. The corrected C–V curves from 6 kHz up to 1 MHz are shown in Figs. 2(c) and 2(d) for samples

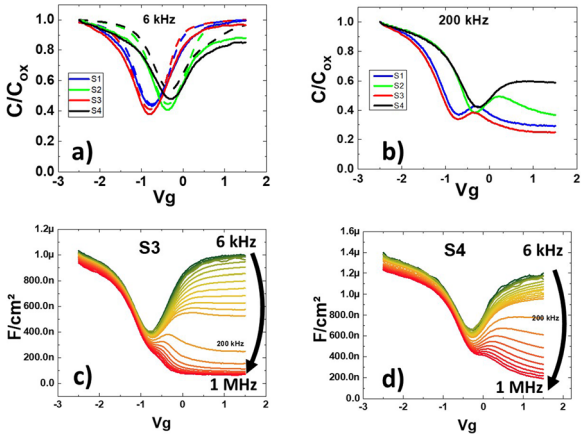

FIG. 2. (a) Normalized *C–V* characteristics (scattered) and simulation (full line) of all samples measured at 6 kHz. (b) Normalized *C–V* characteristics of all samples measured at 200 kHz. Frequency dependence of the corrected *C–V* curves for samples (c) S3 and (d) S4, respectively.

S3 and S4, respectively. The capacitors' gate leakage current does not exceed 5×10^{-6} A cm^{-2} at −2.5 V. The capacitance frequency dispersions measured in accumulation at −2.5 V between 6 kHz and 1 MHz are equal to 9.7%, 7.7%, 11.4%, and 13.9% for samples S1, S2, S3, and S4, respectively. Frequency dispersion is usually caused by border traps near the oxide/semiconductor interface in Ge MOSCAPs.[23,24] Indeed, the presence of traps close to the interface changes the tunneling time constant, resulting in frequency dispersion.[25] In addition, several important parameters can be extracted from these C–V measurements such as the interface state density, the flatband voltage, and the minority carrier generation time. The conductance method, described by Nicollian and Goetzberger,[26] is generally used to extract the interface state density as it provides a precise measurement. However, in the case of a low bandgap material such as GeSn, this method becomes less effective due to the minority carrier response (e^- here) leading to higher uncertainties. Hence, C–V measurements were simulated using a customized analytical C–V model described elsewhere.[20] The model includes a quasicontinuum of interface traps with a constant energy density over the bandgap and minority carrier generation time.

Table II provides the extracted interface state density, the minority carrier generation time (τ_{min}), and the flatband voltage for the various samples. As expected, the sample with no interfacial layer (S4) exhibits a high interface state density, i.e., 6×10^{12} eV^{-1} cm^{-2}. In contrast, samples S1 and S3 with a GeSnOx interfacial layer have the lowest interface state densities, 7×10^{11} eV^{-1} cm^{-2} and 5×10^{11} eV^{-1} cm^{-2}, i.e., values even better than that of sample S2 with an Al_2O_3 IL having a D_{it} of 9×10^{11} eV^{-1} cm^{-2}. However, the interfacial layer does not affect only the interface quality. Indeed, all samples have different minority carrier generation times, as seen on the normalized C–V curves at 200 kHz in Fig. 2(b). The minority carrier generation times (τ_{min}) were simulated in our model with the following expression:

$$C_{min}(\tau_{min}) = \frac{C_{min}}{1 + (2\pi * f * \tau_{min})^2}, \quad (4)$$

where C_{min} is the quasistatic minority carrier capacitance. The samples with $GeSnO_x$ at the interface (S1 and S3) present similar values of ≈9 μs. The sample with Al_2O_3 (S2) has a shorter minority generation time $\tau_{min} = 7$ μs. The minority carrier generation time is the fastest in the sample without any interlayer (S4), with $\tau_{min} = 4$ μs only. Schulte-Braucks *et al.*[27] studied the inversion response as a function of the Sn content in metal/high-k/GeSn MOS capacitors. They showed that higher Sn contents resulted in higher minority carrier generation times. The different τ_{min} in our samples could be explained by interfacial tin concentration differences depending on the interlayer used although the same GeSn layer was used for all MOS capacitors. The GeSn lattice at the interface is apparently modified during the ALD process.

Finally, it should be noted that nonoxidized samples S2 and S4 exhibit Vfb values close to those of the ideal ones ≈−0.61 V.[28]

TABLE II. Extracted parameters of all samples from the C–V simulations.

	S1	S2	S3	S4
D_{it} (eV^{-1} cm^{-2})	7×10^{11}	9×10^{11}	5×10^{11}	6×10^{12}
τ_{min} (μs)	8.5	7	9	4
Vfb (V)	−1.2	−0.8	−1.2	−0.6

Instead, oxidized samples S1 and S3 show more negative Vfb values due to extra positive charges or compensation of the existing negative charges. Indeed, S. Gupta *et al.*[29] investigated the $GeSnO_2/Ge_{0.92}Sn_{0.08}$ and $GeO_2/Ge_{0.92}Sn_{0.08}$ interfaces by deep level transient spectroscopy (DLTS) and saturation photovoltage (SPV). In the case of the $GeSnO_2$/GeSn interface, they demonstrated that the majority of the traps were positively charged close to the valence band edge. Given the global decrease of D_{it} when $GeSnO_x$ is used, it can be deduced that surface oxidation prior to high-*k* deposition does neutralize the existing negatively charged traps. It should also be mentioned that, in our samples, no significant hysteresis was observed during the forward and backward gate voltage sweep, indicating that border traps have no major impact in both oxidized and nonoxidized cases.

To better understand the electrical behavior of each GeSn pMOS capacitor, an in-depth investigation of the chemical composition and the different oxidation states of each compound at the dielectric/GeSn interface is necessary. For this, the XPS experiments were carried out on four dedicated samples using the same conditions as described in Table I. The four samples consist of 2 nm of Al_2O_3, 2 nm of HfO_2, 2 nm of $GeSnO_x$ on $Ge_{0.9}Sn_{0.1}$, and 2 nm of $HfO_2/GeSnO_x/Ge_{0.9}Sn_{0.1}$, called I1, I2, I3, and I_4, respectively. Calibration of the XPS spectra was done by using the main C1s peak at 285 eV of the adventitious carbon which is adsorbed on the samples surface during the transfer, and all recorded XPS peaks were fitted using a Shirley background.

Figure 3 shows the fitted Ge3d and Sn3d peaks of I1-I3 samples. The Ge3d peak fitting of different samples shows the presence of

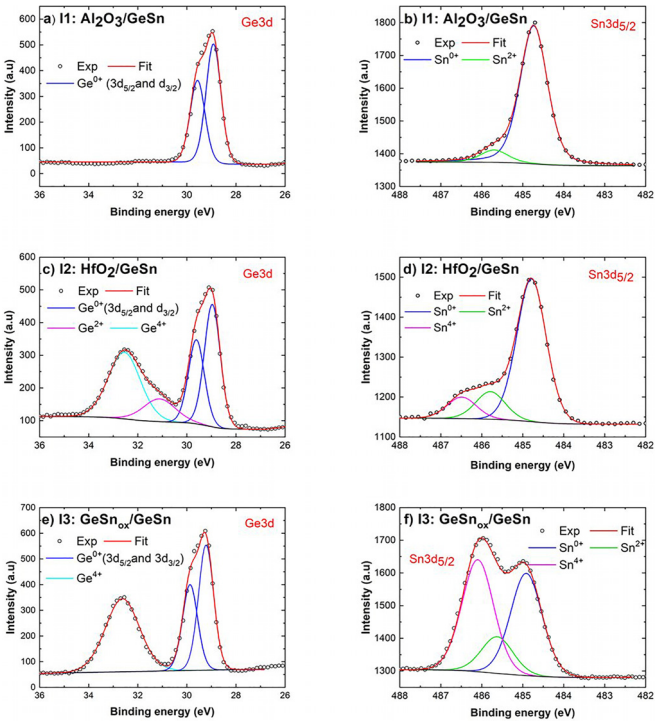

FIG. 3. XPS spectra [(a), (c), and (e)] of Ge3d and [(b), (d), and (f)] $Sn3d_{5/2}$ for I1(Al_2O_3/GeSn10%), I2(HfO_2/GeSn10%), and I3($GeSnO_x$/GeSn 10%), respectively.

$Ge3d_{3/2}$ and $Ge3d_{5/2}$ peaks at 28.7 and 29.7 eV, which are the signature of Ge in the GeSn layer. Likewise, the tin (Sn) spectra of all samples show a peak at 484.8 eV, $Sn3d_{5/2}$, which is attributed to the Sn atoms in the $Ge_{0.9}Sn_{0.1}$ layer. For I1, XPS reveals the absence of Ge oxidation states [Fig. 3(a)] and shows a small peak at 485.6 eV [Fig. 3(b)] associated with the Sn^{2+} state corresponding to the Sn-O bond. The latter highlights a good compatibility between Al_2O_3 and $Ge_{0.9}Sn_{0.1}$ and a high interface quality. For I2, there are two additional subpeaks, shifted from the Ge3d peak by 1.7 and 3.5 eV toward higher binding energies [Fig. 3(c)]. These peaks are attributed to the Ge^{2+} and Ge^{4+} states, which correspond to GeO and GeO_2, respectively. Moreover the $Sn3d_{5/2}$ [Fig. 3(d)] shows the presence of two peaks at 485.6 and 486.1 eV, corresponding to the Sn^{2+} and Sn^{4+} states, respectively. These results indicate the low quality of the $HfO_2/Ge_{0.9}Sn_{0.1}$ interface due to the presence of a mixture of different oxides. Moreover, I2 contains GeO which is known to be volatile. For I3, only the Ge^{4+} state corresponding to the Ge-O_2 bond was detected [Fig. 3(e)]. The $Sn3d_{5/2}$ [Fig. 3(f)] shows the presence of an intense peak at 486.2 eV corresponding to the Sn^{4+} state and a relatively small peak at 486.1 eV attributed to the Sn^{2+}. Thus, these results show the chemical homogeneity of the $GeSnO_x$ layer, with a domination of 4+ states for Ge and Sn, which corroborates the lower value of Dit of 5×10^{11} eV^{-1} cm^{-2} measured for sample S3. For I4, XPS measurements (not presented here) show the same behavior of the $GeSnO_x$ layer as I3.

To summarize, the XPS results demonstrate that the $GeSnO_x$/GeSn interface is chemically stable in I1, I3, and I4 samples. However, I2 ($HfO_2/Ge_{0.9}Sn_{0.1}$) has a mixture of Ge and Sn oxidation states, likely due to a reaction between HfO_2 precursors and the GeSn surface during the ALD of HfO_2. To clarify these points, pAR-XPS experiments were performed on I1-I4 samples. Hf4d, Ge3d, $Sn3d_{5/2}$, Al2p, and O1s spectra were recorded at emission angles from 23.5° to 75.25° with respect to the normal of the sample. Using these spectra, the composition depth profiles of I1-I3 were calculated using the Avantage® software based on the maximum entropy method.[30,31]

Figure 4 shows the in-depth chemical profiles of I1 [Fig. 4(a)], I2 [Fig. 4(b)], I3 [Fig. 4(c)], and I4 [Fig. 4(d)], respectively. Regardless of the sample, the GeSn composition is in a good agreement with the expected value (90% Ge and 10% Sn). For I1, the stoichiometry of the Al_2O_3 layer is the expected one, with Ge_{ox} or Sn_{ox} below the detection limit at the interface. This result explains the low D_{it} value obtained on S2 (see Table II). For I2, the depth profile shows a diffusion of Ge_{ox} within the HfO_2 layer. Such a behavior was already reported for HfO_2/Ge or SiGe by several groups[32–34] and could be responsible for the dielectric permittivity, leakage current, and interface state density issues.[35] In the case of GeSn, Ge diffusion into the HfO_2 layer results in a modification of the $Ge_{1-x}Sn_x$ stoichiometry close to the interface and, thus, a Sn segregation. This hypothesis is well supported by CV measurements and the theoretical simulations which give a higher D_{it} value (see Table II). In the I3 sample case, the chemical profile shows the chemical stoichiometry of $GeSnO_2$ perfectly. Moreover, the I4 depth profile [Fig. 4(d)] does not reveal any intermixing of HfO_2 with the Ge or Sn compound which provides evidence that in the case of $GeSnO_x$ passivation, the interface is stable and the Ge out-diffusion is suppressed.

The pAR-XPS results are in a agreement with the Dit values (Table II) which shows that the sample with $GeSnO_x$ and Al_2O_3 interface layers has a lower Dit. The superiority of the $GeSnO_x$/GeSn compared to the Al_2O_3/GeSn interface can be explained by the fact that the

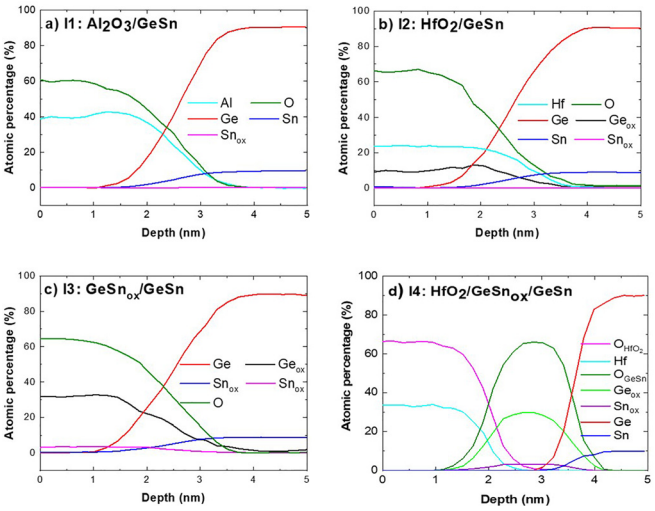

FIG. 4. Chemical depth profiles of (a) I1 (Al_2O_3/GeSn), (b) I2 (HfO_2/GeSn), (c) $GeSn_{ox}$/GeSn, and (d) I4 ($HfO_2/GeSn_{ox}$/GeSn). The relative concentrations of aluminum (Al), hafnium (Hf), germanium (Ge), tin (Sn), germanium oxide (Ge_{ox}), tin oxide (Sn_{ox}), and oxygen are plotted as functions of depth.

$GeSnO_x$ layer ensures a natural chemical continuity with the GeSn surface which is not the case with Al_2O_3.

The use of interlayers in HfO_2/GeSn p-MOS capacitors was investigated in order to improve their electrical performance. It was found that the direct deposition of HfO_2 by ALD on GeSn resulted in Ge diffusion through the HfO_2 layer, altering the semiconductor and dielectric properties and leading to a high interface state density. We showed that the *in situ* formation of an interlayer $GeSnO_x$ layer prevented the intermixing of HfO_2 and Ge. It was found that the use of this interlayer drastically reduced the interface state density, with the obtained values as low as 5×10^{11} eV^{-1} cm^{-2}. These findings are of critical importance for the fabrication of future high mobility MOS transistors with GeSn channels.

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